TIPS FOR A BETTER LAB SESSION

Some of the Best Practices to help the Lab run smoothly while maximizing Student Learning.

1. Students should be thoroughly familiar with the Lab exercises before coming to Lab.
2. Students should treat the Laboratory Exercises as original Research.
3. Students should make sure not to miss even a single Lab Class.
4. Students must apply the concepts learned in class to New Situations.
5. Each student must try to do their Lab Exercises Individually.
6. The instructor will hold a pre-laboratory discussion on the lab exercises.
7. Before every lab session each student should draw the circuit diagram for the lab exercise, write the purpose of each component in the circuit and its application in the empty space provided.
8. Each student must be able to design the circuit for the specifications given during the lab session.
9. Students are encouraged to do the additional lab exercise provided in the manual. Extra credit will be awarded for the same.
10. The progress of every student will be monitored on a regular basis. Based on the progress report Extra Credit Marks will be awarded for the students in their Internals.
11. Every student must be able to explain the circuit, its functioning and application clearly at the end of each Lab Session.
12. Labs are for you students and so consider it as your duty to leave the lab exactly how you found it, by taking care of the computer systems and the other equipments.

"ENJOY THE JOY OF DESIGNING"

ANNA UNIVERSITY, CHENNAI
SYLLABUS(R 2013)

EC6411 CIRCUITS AND SIMLATION INTEGRATED LAB

DESIGN AND ANALYSIS OF THE FOLLOWING CIRCUITS

1. Series and Shunt feedback amplifiers-Frequency response, Input and output impedance- calculation
2. RC Phase shift oscillator and Wien Bridge Oscillator
3. Hartley Oscillator and Colpitts Oscillator
4. Single Tuned Amplifier
5. RC Integrator and Differentiator circuits
6. Astable and Monostable multivibrators
7. Clippers and Clampers
8. Free running Blocking Oscillators

SIMULATION USING SPICE (Using Transistor):

1. Tuned Collector Oscillator
2. Twin -T Oscillator / Wein Bridge Oscillator
3. Double and Stagger tuned Amplifiers
4. Bistable Multivibrator
5. Schmitt Trigger circuit with Predictable hysteresis
6. Monostable multivibrator with emitter timing and base timing
7. Voltage and Current Time base circuits

LIST OF EXPERIMENTS

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2.	Twin -T Oscillator	111
3.	Wein Bridge Oscillator	115
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SIMULATION

Ex. No	DATE	TITLE OF THE EXPERIMENT	PAGE No.	MARKS (30)	SIGNATURE OF THE FACULTY
1.					
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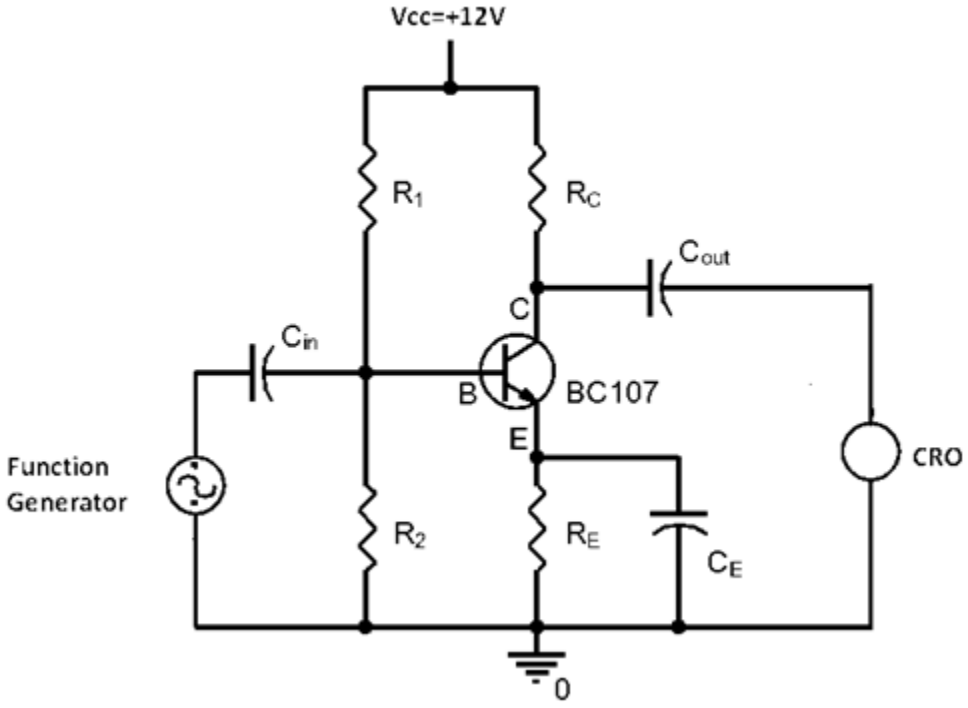
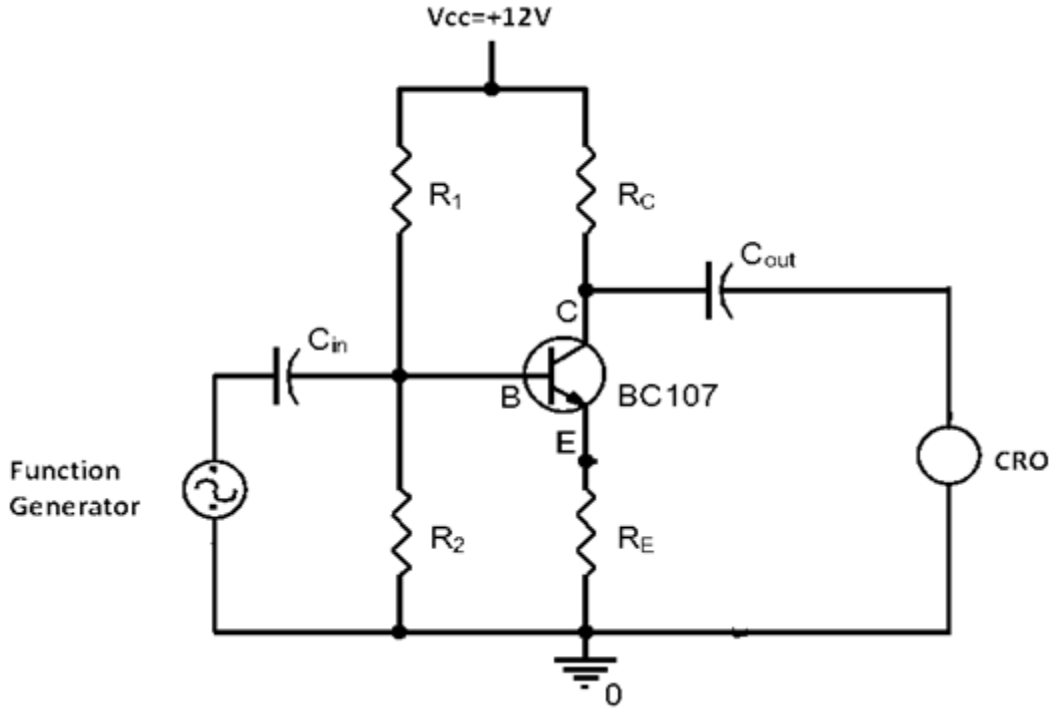
SIGNATURE OF THE FACULTY **TOTAL MARKS(30):**

CIRCUIT DIAGRAM

CURRENT SERIES FEEDBACK AMPLIFIER (WITHOUT FEEDBACK)



CURRENT SERIES FEEDBACK AMPLIFIER (WITH FEEDBACK)



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Date:

CURRENT – SERIES FEEDBACK AMPLIFIER
(TRRANSCONDUCTACNE AMPLIFER)

AIM

To design the current series feedback amplifier and calculate the following parameters with and without feedback condition.

1) Mid-band gain
2) Cut-off frequency
3) Bandwidth
4) Input impedance
5) Output impedance

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Function Generator	(0-2)MHz	1
3.	Transistor	BC 107	1
4.	Resistor		
5.	Capacitor		
6	Bread board	-	1
7	Power supply	(0-30)V	1

THEORY

An ideal amplifier provides a stable output which is an amplified version of the input signal. But the gain and stability of this amplifier are not consistent due to changes in ambient temperature, parameter variation and non linearity in the device. This problem is overcome by the techniques of feedback, wherein a portion of the output signal in feedback to the input and combined with the input signal to produce the desired output.

The feedback may be classified into two types:

1) Positive feedback
2) Negative feedback

DESIGN

Given V_{cc}=12V, I_c=I_e=2mA, V_{be}=0.7,

$h_{fe} = \beta$=

$V_{ce} = V_{cc}/2$

$V_e = V_{cc}/10$;

$r_e = 26mV/I_e$

$R_e = V_e/I_e$

Calculating R_C value:

Apply KVL to output circuit

$V_{cc} = I_cR_c + V_{ce} + I_eR_e$

⇨ $R_c = (V_{cc} - V_{ce} - I_eR_e)/I_c$

Calculating R_{b1} and R_{b2} value:

$V_B = V_{BE} + V_E$,

Assume (R_{b2} =10KΩ)

$$\text{W.k.t ., } V_B = \frac{V_{CC}.Rb_2}{Rb_1 + Rb_2}$$

$R_{b1} = [(V_{cc} * R_{b2})/(V_B)] - R_{b2}$

Calculating input coupling capacitor:

$Xci = [h_{ie} + (1+h_{fe})R_e] \,||\, R_b)\,]/10$

$R_b = R_{b1} || R_{b2} = (R_{b1} * R_{b2})/(R_{b1} + R_{b2})$

$h_{ie} = h_{fe} * r_e$

$C_i = 1/(2\pi f X_{ci})$ assume f =50Hz

Assume output coupling capacitor

C_o = 10μf

Calculating Emitter Bypass Capacitor:

$X_{ce} = R_e/10$

$C_e = 1/(2\pi f X_{ce})$ assume f =50Hz

a) **Positive feedback**

If the feedback signal applied is in phase with the input signal, it results in increase in the input and is called as positive feedback or regenerative feedback. The voltage gain of a feedback is greater than the open loop gain.

b) **Negative feedback**

If the feedback signal applied to the input is out of phase with the input signal then the net input signal to the amplifier decreases. This is known as negative feedback or degenerative feedback.

The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased. In Current-Series Feedback, the input impedance and the output impedance are increased. Noise and distortions are reduced considerably.

Trans conductance:

In a current series feedback amplifier the sampled signal is a current and the feedback signal (Which is fed in series)is a voltage.

$$Gm = I_o / Vi$$

Where

Gm = Amplifier gain.
I_o = Output current.
Ii = Input current.

Block diagram:

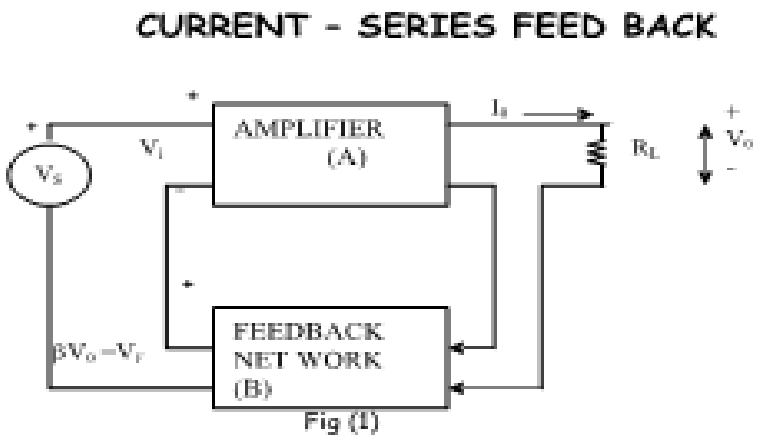


Fig (1)

Theoretical amplifier parameter calculation

Voltage gain $A_v = -V_o/V_i$

Without feedback

Voltage gain $A_v = -R_c/ [(R_e||X_{ce})+r_e]$
Input impedance $Z_i = R_b || (R_e+r_e)\beta$
Output impedance $Z_o=R_c$
Transconductance $G_m= -h_{fe}/(h_{ie}+R_e)$

With feedback

Voltage gain with feedback $A_{vf} = -R_c/(R_e+r_e)$

Feedback factor $\beta_f = -R_e$
Desensitivity $D = 1+ (\beta_f * G_m)$
Transconductance with feedback $G_{mf} = G_m/D$
Input impedance $Z_{if} = R_b || ((R_e||X_{ce})+r_e)\beta$
Output impedance $Z_{of}=R_c$

Amplifier

When high input and output impedance and finite gain are required. The CurrentSeries feedback is employed. Fig shows a current series amplifier block diagram. It can be seenthat a current series feedback amplifier results in, when the emitter bypass capacitor of the common emitter amplifier is removed.

Typical value of gain for this single stage would be around 5 to 10 0nly, with openloop gain ranging from 100 to 300. To get higher values of gain, single stage amplifiers canbe connected in cascade.

Feedback network:

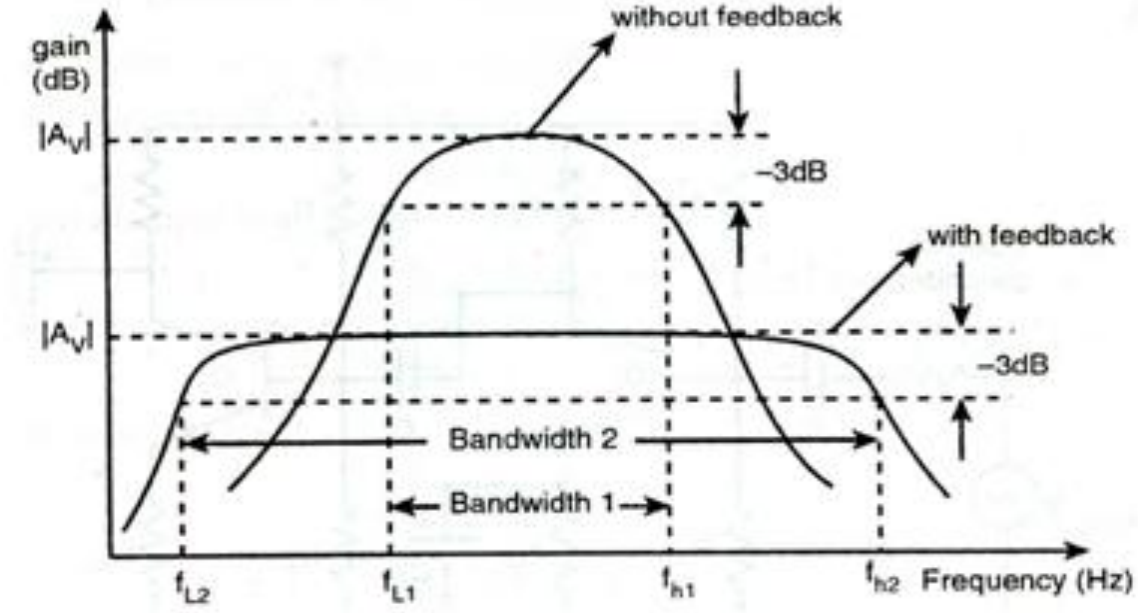
To construct an amplifier with precise gain we must employ negative feedbackTechniques. This makes the gain to be independent of β and dependent only on the characteristics of the feedback network. Usually resistors are used to
Construct feedback networks.

Effect of Feedback

- ✓ Output resistance: increases
- ✓ Input resistance: increases
- ✓ Gain: Trans conductance amplifier: decreases
- ✓ Bandwidth: increases
- ✓ Distortion: Decreases

MODEL GRAPH

Model Graph (Frequency Response) :-



PROCEDURE

Without feedback

1. Connect the circuit as per the circuit diagram.
2. Set Vs = 50mV (say) at f=1KHz (this is for checking purpose) using signal generator. Keeping the input voltage constant vary the frequency from 10Hz to 1MHz in regular
3. Steps and note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.

With feedback

1. Remove the emitter bypass capacitor.
2. Set Vs = 50mV (say) at f=1KHz (this is for checking purpose) using signal generator.
3. keeping the input voltage constant vary the frequency from 10Hz to 1MHz in regular
4. Steps and note down the corresponding output voltage.
5. Plot the Graph: gain (dB) Vs frequency.
6. Calculate the bandwidth from Graph.

To find input impedance

1) Open circuit the output port and connect DRB (Decade Resistance Box) between function generator and input coupling capacitor. CRO output taken after DRB.
2) The input signal V_s = 1v is set at f=1 KHz.
3) The DRB is adjusted and V_{in}=0.5V (half the input voltage) is brought. The value shown by the DRB gives the input impedance.
4) The same procedure repeated foe circuit with feedback

To find output impedance

1) Short circuit the input port and connect the DRB across the coupling capacitor. CRO output is taken across DRB
2) The input signal V_s = 1v is set at f=1 KHz.
3) The DRB is adjusted and V_{in}=0.5V (half the input voltage) is brought. The value shown by the DRB gives the output impedance.
4) The same procedure repeated foe circuit with feedback

TABULATION: V_{in}=

S.No.	With FB			Without FB		
	Frequency (Hz)	Output Voltage (Volts)	Gain = $20\log(V_o/V_i)$ (dB)	Frequency (Hz)	Output Voltage (Volts)	Gain = $20\log(V_o/V_i)$ (dB)

REVIEW QUESTIONS:

1. What is Feedback?
2. What are the types of feedback in amplifier?
3. What is Negative feedback?
4. Differentiate Negative feedback and Positive feedback.
5. What are the types of negative FB is used in amplifiers?
6. Give any four merits of negative FB?
7. Define desensitivity?

RESULT

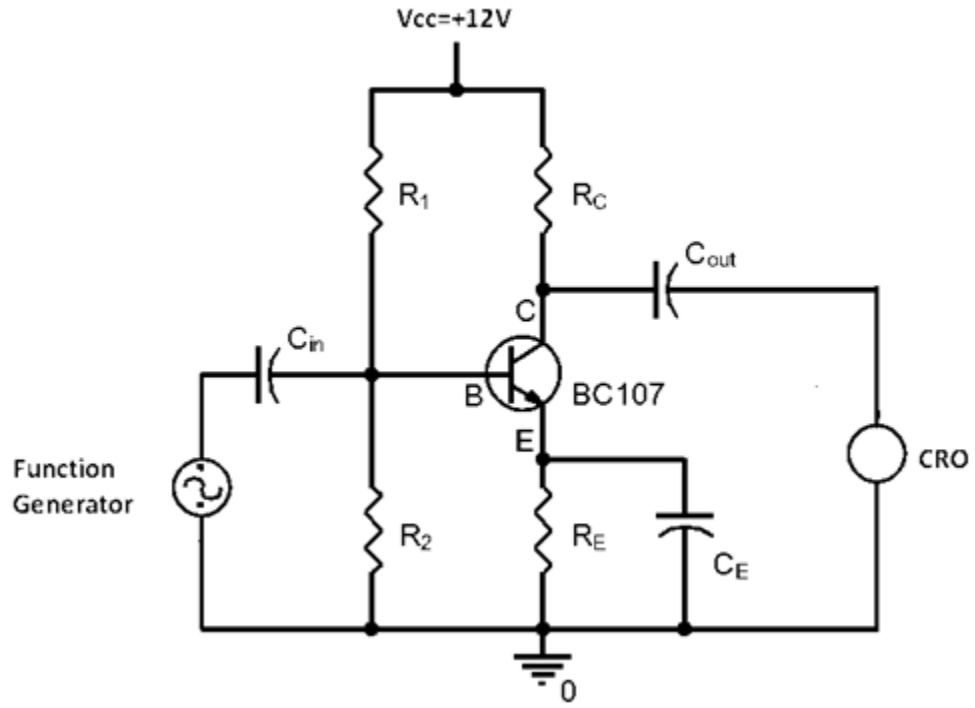
Thus the current series feedback amplifier is designed and the following results are obtained.

Parameter	Theoretical		Practical	
	With feedback	Without feedback	With feedback	Without feedback
Mid band gain				
Lower cut off frequency (f_L)				
Upper cut off frequency (f_H)				
Bandwidth				
Input impedance				
Output impedance				

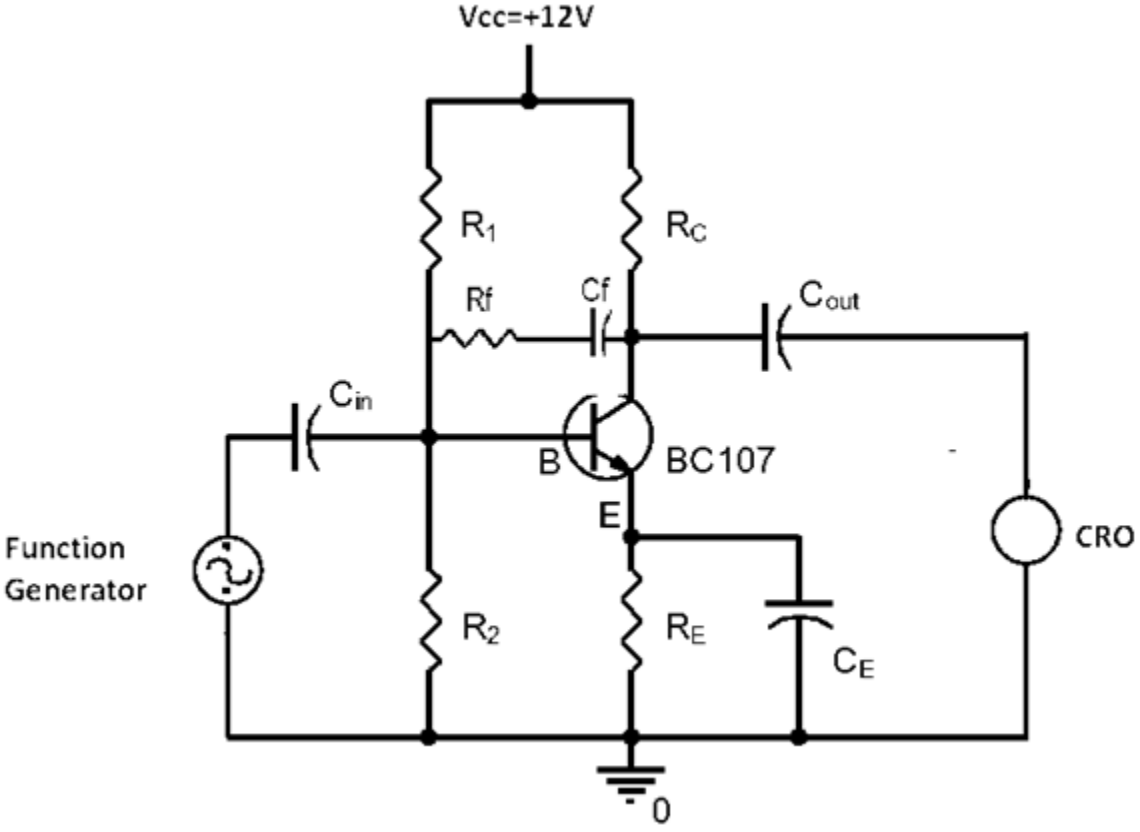
MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

CIRCUIT DIAGRAM

VOLTAGE SHUNT FEEDBACK AMPLIFIER (WITHOUT FEEDBACK)



VOLTAGE SHUNT FEEDBACK AMPLIFIER (WITH FEEDBACK)



Ex. No:
Date:

VOLTAGE SHUNT FEEDBACK AMPLIFIER
(TRANSRESISTANCE AMPLIFIER)

AIM

To design the Voltage shunt feedback amplifier and calculate the following parameters with and without feedback condition.

1. Mid-band gain
2. Cut-off frequency
3. Bandwidth
4. Input impedance
5. Output impedance

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Function Generator	(0-2)MHz	1
3.	Transistor	BC 107	1
4.	Resistor		
5.	Capacitor		
6	Bread board	-	1
7	Power supply	(0-30)V	1

THEORY

An ideal amplifier provides a stable output which is an amplified version of the input signal. But the gain and stability of this amplifier are not consistent due to changes in ambient temperature, parameter variation and non linearity in the device. This problem is overcome by the techniques of feedback, wherein a portion of the output signal in feedback to the input and combined with the input signal to produce the desired output.

The feedback may be classified into two types:

1) Positive feedback

2) Negative feedback

DESIGN

Given V_{cc}=12V, I_c=I_e=2mA, V_{be}=0.7, h_{fe} = β=

V_{ce}= V_{cc}/2

V_e=V_{cc}/10;

r_e=26mV/I_e

R_e=V_e/I_e

Calculating R_C value:

Apply KVL to output circuit

V_{cc}= I_cR_c+V_{ce}+I_eR_e

⇨ R_c=(V_{cc}-V_{ce}-I_eR_e) /I_c

Calculating R_{b1} and R_{b2} value:

$V_B = V_{BE} + V_E$,

Assume (R_{b2} =10KΩ)

W.k.t, $V_B = \frac{V_{CC}.Rb_2}{Rb_1 + Rb_2}$

R_{b1} = [(V_{cc} * R_{b2})/ (V_B)] −R_{b2}

Calculating input coupling capacitor:

Xci = [h_{ie} +(1+h_{fe}) R] || R_b)] /10

R_b = R_{b1}|| R_{b2} = (R_{b1}*R_{b2}) / (R_{b1}+R_{b2})

h_{ie} =h_{fe}*r_e

C_i=1 /(2πfX_{ci}) assume f =50Hz

Assume output coupling capacitor

C_o = 10μf

Calculating Emitter Bypass Capacitor:

X_{ce} =R_e/10

C_e = 1 /(2πfX_{ce}) assume f =50Hz

a) **Positive feedback**

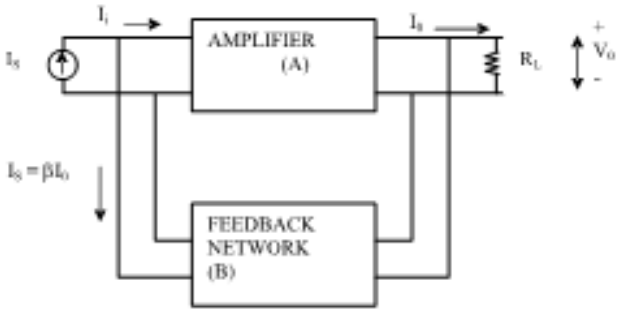
If the feedback signal applied is in phase with the input signal, it results in increase in the input and is called as positive feedback or regenerative feedback. The voltage gain of a feedback is greater than the open loop gain.

b) **Negative feedback**

If the feedback signal applied to the input is out of phase with the input signal then the net input signal to the amplifier decreases. This is known as negative feedback or degenerative feedback.

Block diagram:

Voltage Shunt Feedback amplifier



Transresistance:

In voltage shunt feedback amplifier the sampled signal is a voltage and the feedback signal (Which is fed in shunt) is a current.

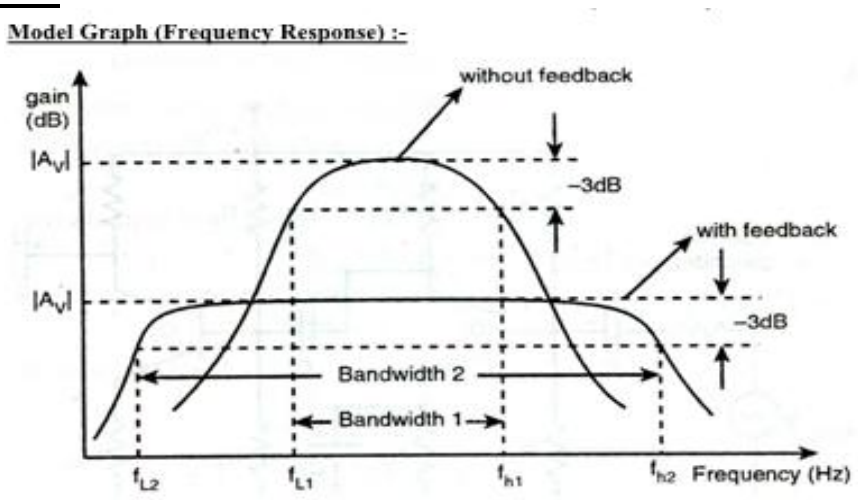
$Rm = V_o / Ii$ (or) $V_o = Rm.\ Ii$

Where Rm = Amplifier gain.
V_o = Output voltage.
Ii = Input current.

Effects of voltage shunt feedback:

- ✓ Output resistance: decrease
- ✓ Input resistance: decrease
- ✓ Gain: Trans conductance amplifier: decreases
- ✓ Bandwidth: increases
- ✓ Distortion: Decreases

MODEL GRAPH



Theoretical amplifier parameter calculation:

Voltage gain $Av = -V_o/V_{in}$

Without feedback

Voltage gain $Av = -R_c / [(R_e || X_{ce}) + r_e]$

Input impedance $Z_i = R_b || (R_e + r_e)\beta$ where $\beta = h_{fe}$

Output impedance $Z_o = R_c$

With feedback

Feedback factor $\beta_f = -1/R_f$

Voltage gain with feedback $A_{vf} = A_v / (1 + A_v \beta_f)$

Input impedance $Z_{if} = Z_i / (1 + A_v \beta_f)$

Output impedance $Z_{of} = Z_o / (1 + A_v \beta_f)$

PROCEDURE

Without feedback

1. Connect the circuit as per the circuit diagram.
2. Set Vs = 50mV (say) at f=1KHz (this is for checking purpose) using signal generator. Keeping the input voltage constant vary the frequency from 10Hz to 1MHz in regular
3. Steps and note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.

With feedback:

1. Insert the feedback resistor and capacitor between base and collector
2. Set Vs = 50mV (say) at f=1KHz (this is for checking purpose) using signal generator.
3. keeping the input voltage constant vary the frequency from 10Hz to 1MHz in regular
4. Steps and note down the corresponding output voltage.
5. Plot the Graph: gain (dB) Vs frequency.
6. Calculate the bandwidth from Graph.

To find input impedance:

1. Open circuit the output port and connect DRB (Decade Resistance Box) between function generator and input coupling capacitor. CRO output taken after DRB.
2. The input signal V_s = 1v is set at f=1 KHz.
3. The DRB is adjusted and V_{in}=0.5V (half the input voltage) is brought. The value shown by the DRB gives the input impedance.
4. The same procedure repeated foe circuit with feedback

To find output impedance:

1. Short circuit the input port and connect the DRB across the coupling capacitor. CRO output is taken across DRB
2. The input signal V_s = 1v is set at f=1 KHz.
3. The DRB is adjusted and V_{in}=0.5V (half the input voltage) is brought. The value shown by the DRB gives the output impedance.
4. The same procedure repeated foe circuit with feedback

TABULATION:

V_{in}=

S.No.	With FB			Without FB		
	Frequency (Hz)	Output Voltage (Volts)	Gain = $20\log(V_o/V_i)$ (dB)	Frequency (Hz)	Output Voltage (Volts)	Gain = $20\log(V_o/V_i)$ (dB)

RESULT

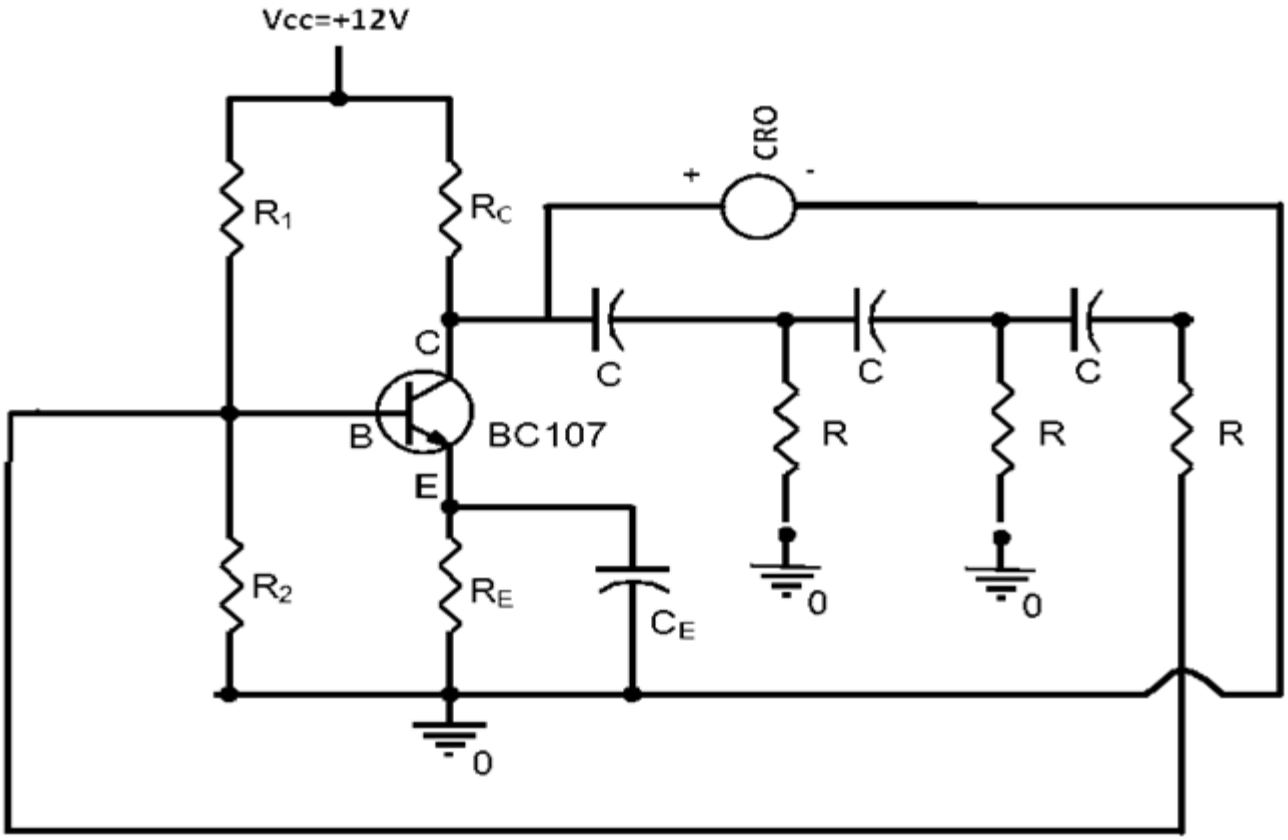
Thus the Voltage shunt feedback amplifier is designed and the following results are obtained.

Parameter	Theoretical		Practical	
	With feedback	Without feedback	With feedback	Without feedback
Mid band gain				
Lower cut off frequency (f_L)				
Upper cut off frequency (f_H)				
Bandwidth				
Input impedance				
Output impedance				

MARKS ALLOCATION		
Experimental Setup	10	
Execution	10	
Viva	10	
Total	30	

CIRCUIT DIAGRAM

RC PHASE SHIFT OSCILLATOR



Ex. No:
Date:

RC PHASE SHIFT OSCILLATOR

AIM

To design, construct and obtain the oscillations of RC Phase shift oscillator.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1	CRO	(0-30) MHz	1
2	Transistor	BC 107	1
3	Power supply (RPS)	(0-30)V	1
4	Resistor		
5	Capacitor		
6	Bread board	-	1

THEORY

PHASE SHIFT OSCILLATOR

The circuit arrangement of a phase shift oscillator using NPN transistor in CE configuration consists of, the voltage divider R_1- R_2 which provides the DC emitter bias. R_E and C_E combinations provide temperature stability and prevent AC signal degeneration and collector resistor R_C controls the collector voltage. The oscillator output voltage is coactively coupled to the load by C_C.

In case of a transistor phase shift oscillator, the output of the feedback network is loaded appreciably by the relatively small input resistance (h_{ie}) of the transistor. Hence instead of employing voltage series feedback, voltage shunt feedback is used for a transistor phase shift oscillator. In this circuit, the feedback signal is coupled through the feedback resistor R' in series with the amplifier stage input resistance h_{ie}. The value of R' should be such that when added with the amplifier stage input resistance h_{ie} it is equal to R i.e., $R' + h_{ie} = R$.

DESIGN:

PHASE SHIFT OSCILLATOR

Feedback Network:

$F = 1/(2\pi RC\sqrt{(6+4(R_C/R))})$

Let, $R = 5\ K\Omega$ $R_C = 2\ K\Omega$ $F = 5\ KHz$

$\Rightarrow 5 \times 10^{3} = 1/(2\pi\ 5 \times 10^{3} \times C \times \sqrt{(6+(4 \times 2 \times 10^{3}/5 \times 10^{3}))})$

$\Rightarrow C = 0.0023\ \mu F$

Biasing Network Design:

$V_{CE} < V_{CC}/2$

$V_{CE} < 10/2$

$\Rightarrow V_{CE} = 4V$

Kirchhoff's Voltage law for output circuit:

$V_{CC} - V_{CE} = I_C R_C + I_E R_E$ $I_C \approx I_E = 2\ mA$

$\Rightarrow 10 - 4 - I_C(R_C + R_E) = 0$

$\Rightarrow R_C + R_E = 6 \times 10^{3}/2$

$\Rightarrow$ **$R_E = 1\ K\Omega$**

To find R_1 and R_2:

W.k.t $V_B = V_{CC} * R_2/(R_1 + R_2)$ ----------(1)

Also $V_B = V_{BE} + V_E$

$V_B = 0.7 + 2 = 2.7\ V$ For Silicon Transistor $V_{BE} = 0.7$

From equation (1)

$2.7/10 = R_2/(R_1 + R_2)$ ----------(2)

$S = 1 + (R_B/R_E)$ $(S = 10)$

$\Rightarrow R_B = 9\ K\Omega$

$\Rightarrow R_B = R_1 R_2/(R_1 + R_2)$ ---------- (3)Substituting (2) in (3)

$9 = R_1(0.27)$

$R_1 = 33\ K\Omega$ **$R_2 = 12K\Omega$** **$C_E = 33\mu F$**

RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feedback Networks the output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequencies. Since CE Amplifier produces 180 º phases shift the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations.

PROCEDURE

1. Connections are made as per the given circuit diagram
2. Collector voltage signal is monitored in the CRO.
3. The frequency is calculated from the waveform obtained.
4. Base voltage signal is monitored in the CRO to check for the phase shift.
5. The graphs are plotted for V_{CE} Vs Time and V_{BE} Vs Time.

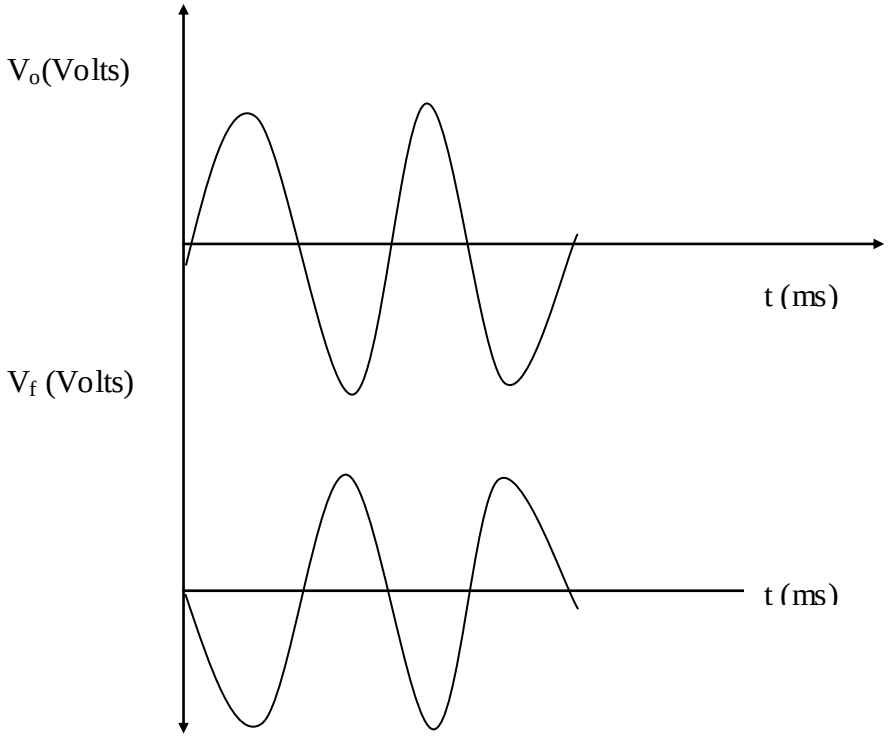
TABULATION

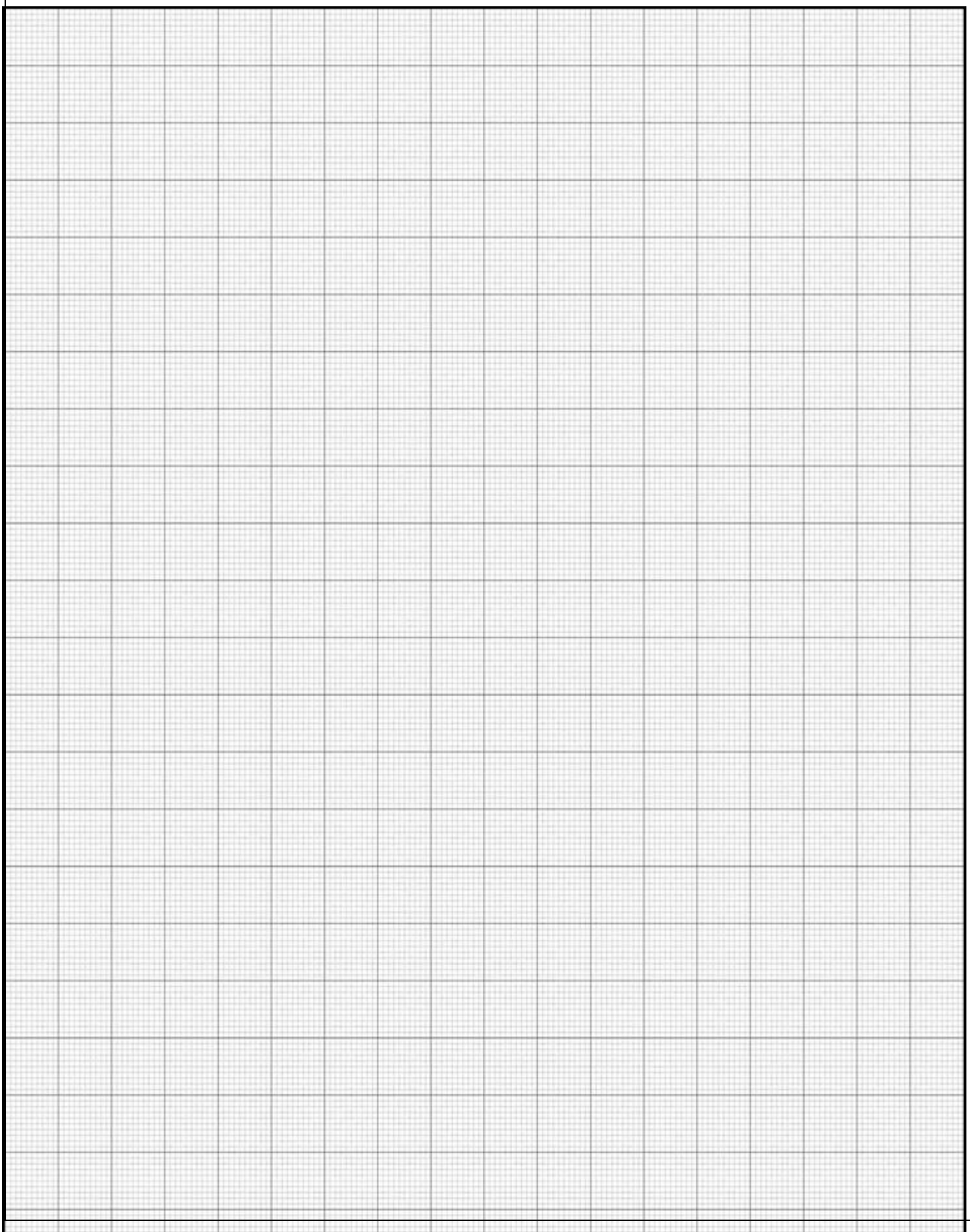
Parameter	(Vo) Across Collector terminal	(V_f) Across Feedback
Amplitude		
Time Period		

MODEL CALCULATION

f = 1 / T =

MODEL GRAPH





REVIEW QUESTIONS:

1. What are the conditions of oscillations?
2. Give the formula for frequency of oscillations?
3. What is the total phase shift produce by the RC ladder network?
4. Whether the oscillator is positive feedback or negative feedback?
5. What is the gain of RC phase shift oscillator?
6. What is the difference between damped oscillations undamped oscillations?
7. What are the applications of RC oscillations?
8. 10. How the Barkhausen criterion is satisfied in RC phase shift oscillator?

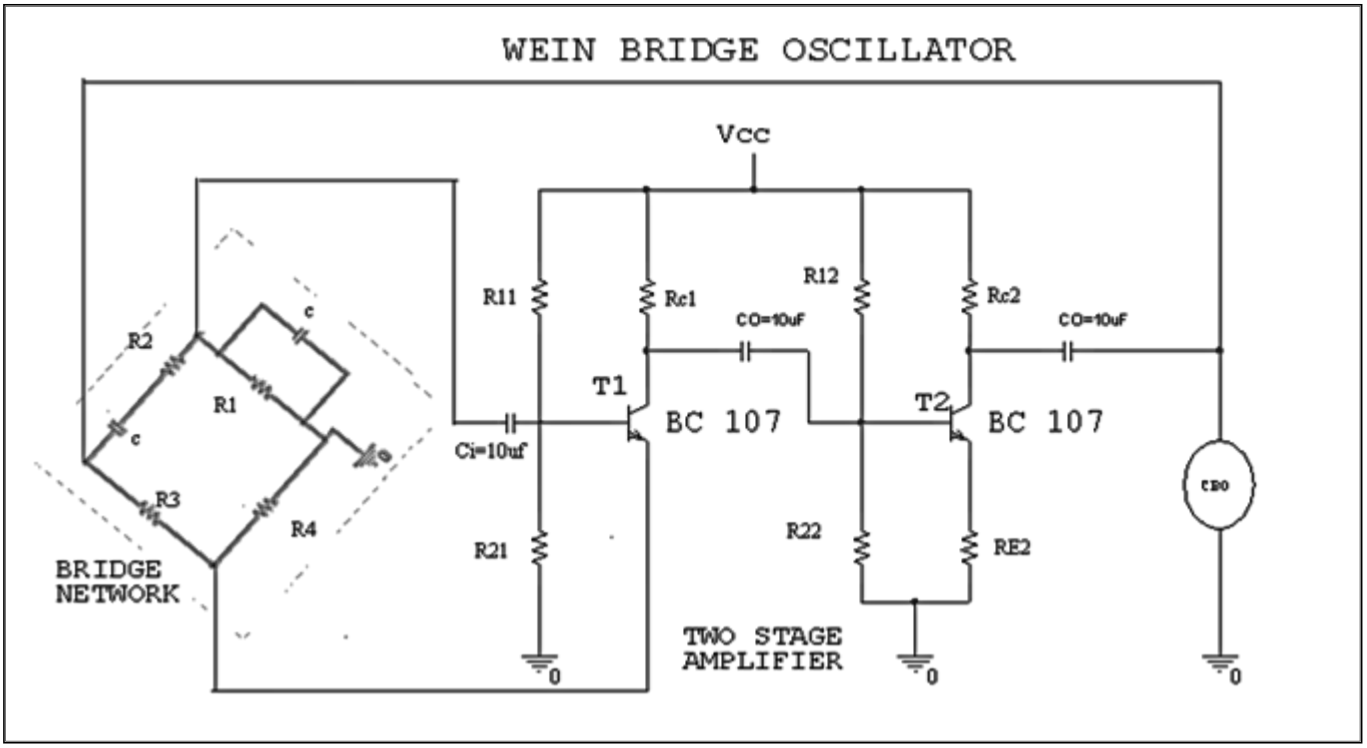
RESULT

Thus the RC Phase shift oscillator is designed and constructed. And also output is verified.

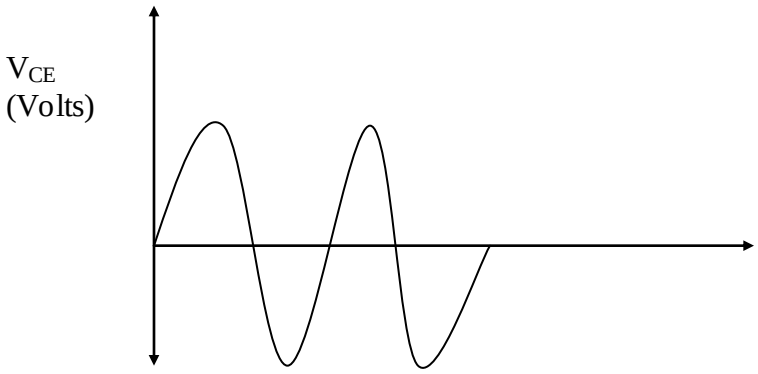
OSCILLATOR	DESIGN FREQUENCY	PRACTICAL FREQUENCY

Marks allocation	
Experimental setup	
execution	
viva	
Total(30)	

CIRCUIT DIAGRAM



MODEL GRAPH



Ex. No:
Date:

WIEN BRIDGE OSCILLATOR

AIM

To design and construct the Wien Bridge oscillator by using transistor. Also obtain 1 KHz oscillation.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Power supply (RPS)	(0-30)V	1
3.	Transistor	BC 107	2
4.	Resistor		
5.	Capacitor		
6	Bread board	-	1

THEORY

The circuit diagram of Wein Bridge oscillator is essentially a two-stage amplifier with an RC bridge circuit. RC bridge circuit (Wein Bridge) is a Lead Lag network. The Phase shift across the network lags with increasing frequency and leads with decreasing frequency. By adding Wein bridge feedback network the oscillator becomes sensitive to a signal of only one particular frequency. This particular frequency is that at which Wein Bridge is balanced and for which the phase shift is 0°.If Wein Bridge feedback network is not employed and output of transistor T_2 is fed back to transistor T_1 for providing regeneration required for producing oscillations, the transistor T_1 will amplify signals over a wide range of frequencies and thus direct coupling would result in poor frequency stability. Thus by employing Wein Bridge feedback network frequency stability is increased.

WEIN BRIDGE OSCILLATOR DESIGN

Frequency of Oscillation:

$fo = (1/2\pi RC)$

Fo =1KHz

$C = 0.01\mu f$

$R= 1/(2\pi fo\ C) = 15.91\ K\Omega$

$Z\ parallel = R \| Xc$; $Xc = 1/2\pi fc$

$Zseries = R + Xc$

$Zf= Zparallel \| Z\ series$

For sustained Oscillations:

$R3 /R4 = 2$

Let, $R3= 100K\Omega$ $R4 =50K\Omega$

Amplifier Stage 1:

$V_{CC} = 12V;$

$I_C=I_E= 4mA;$

$V_{CE}= V_{CC}/2 =6V$

$V_E = V_{CC}/3 =4V;$

$R_E=V_E/I_E = 1K\Omega$

$RC = V_{CC}/ 2\ I_C = 1.5K\Omega$

$(R_{11} \| R_{21}) > 10\ Zf$

So , $R_{11} = 120K\Omega$, $R_{21} =100K\Omega$

Amplifier Stage 2:

$V_{CC} = 12V;$

$I_C=I_E= 1.5mA;$

$V_{CE}= V_{CC}/2 =6V$

$V_E = V_{CC}/10 =1.2V;$

$R_E=V_E/I_E = 800\Omega$

$RC = V_{CC}/ 2\ I_C = 4K\Omega$

$V_B= V_{BE} +V_E = 1.9V$

$V_B= V_{CC} * (R_{22} / (R_{22}+ R_{21})$

$R_{22} = 22K\Omega$

$R_{12} = (V_{CC} * R_{22} /V_B) –R_{22} =116.94\ K\Omega$

PROCEDURE

1. Connections are made as per the given circuit diagram
2. Collector voltage signal of transistor T_2 is monitored in the CRO.
3. The frequency is calculated from the waveform obtained.
4. The graphs are plotted for V_{CE2} Vs Time.

REVIEW QUESTIONS:

1. Give the formula for frequency of oscillations?
2. What is the condition for Wien bridge oscillator to generate oscillations?
3. What is the total phase shift provided by the oscillator?
4. What is the function of lead-lag network in Wien bridge oscillator?
5. Which type of feedback is used in Wien bridge oscillator?
6. What is gain of Wien bridge oscillator?
7. What is the application of Wien bridge oscillator?
8. What is the condition for oscillations?
9. Wien bridge oscillator is either LC or RC oscillator?

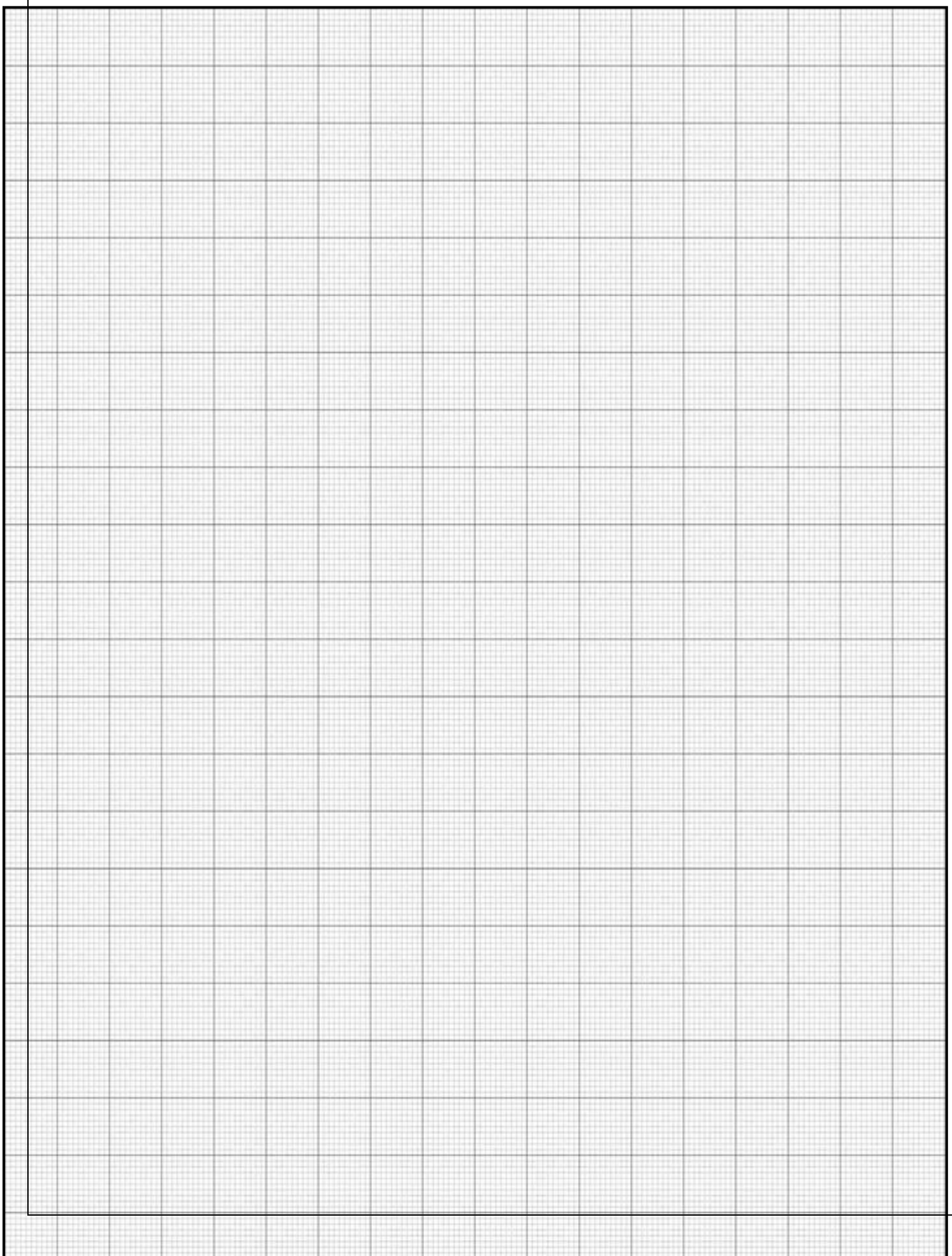
OBSERVATION

S.No	V_{CC} in volts	Vo in Volts	Time in ms	Theoretical Frequency in Hz	Practical Frequency In Hz

MODEL CALCULATION

T =

f = 1 / T =



RESULT

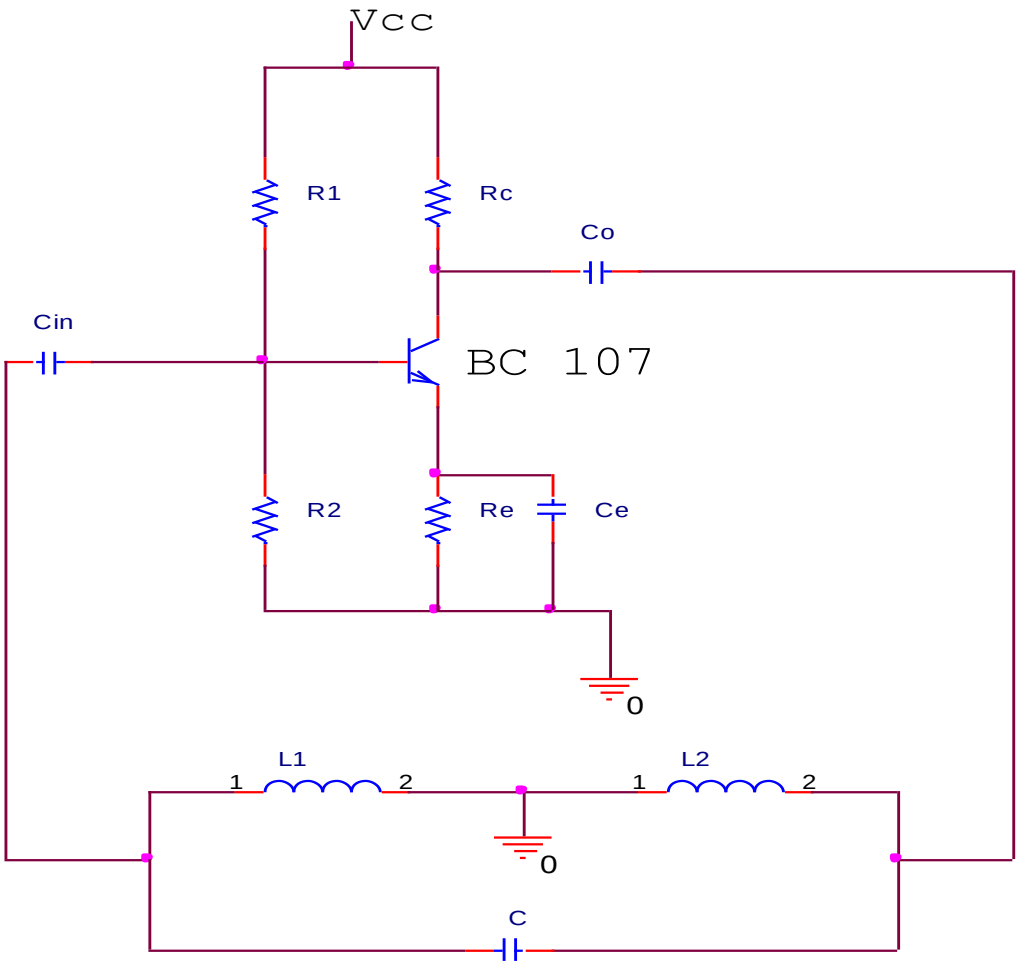
Thus the Wien Bridge oscillator is designed and constructed.

OSCILLATOR	DESIGN FREQUENCY	PRACTICAL FREQUENCY

MARKS ALLOCATION		
Experimental Setup	10	
Execution	10	
Viva	10	
Total	30	

CIRCUIT DIAGRAM

HARTLEY OSCILLATOR



Ex. No:
Date:

HARTLEY OSCILLATOR

AIM

To design a Hartley oscillator to generate sinusoidal signal with a frequency of 325 KHz

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Power supply (RPS)	(0-30)V	1
3.	Transistor	BC 107	1
4.	Resistor		
5.	Capacitor		
6	Bread board	-	1
7	Decade inductance box		1
8	Decade capacitance box		1

THEORY

HARTLEY OSCILLATOR

Hartley oscillator is very popular and is commonly used as a local oscillator in radio receivers. The resistors R_1, R_2 and R_e provide necessary bias conditions for the circuit. Capacitor C_e provides AC ground thereby preventing any signal degeneration.

This also provides temperature stabilization .The frequency determining network is a parallel resonant circuit consisting of inductors L_1 and L_2 and a variable capacitor C .The function of C_C and C_b is to block DC and to provide an AC path.

When the collector supply voltage is switched ON, a transient current is produced in the tank circuit. This oscillatory current in the tank circuit produces AC voltage across L_1.In this way, the feedback between output and input circuits is accomplished through auto transformer action. So there is a phase reversal of 180° between output and input. The common emitter amplifier also produces a further 180° phase shift between input and output voltages. Thus the total phase shift becomes 360°.This makes the feedback positive, which is an essential condition for oscillations.

DESIGN

Biasing Network Design

$V_{CE} < V_{CC} / 2$

$V_{CE} < 10 / 2$

⇨ $V_{CE} = 4V$

Kirchhoff's Voltage law for output circuit:

$V_{CC} - V_{CE} = I_C R_C + I_E R_E$ $\quad I_C \approx I_E = 2$ mA

⇨ $10 - 4 - I_C(R_C + R_E) = 0$

⇨ $R_C + R_E = 6 \times 10^3 / 2$

⇨ **$R_E = 1$ KΩ**

To find R_1 and R_2

$V_B = V_{CC} R_2 / (R_1 + R_2)$ ----------(1)

Also $V_B = V_{BE} + V_E$

$V_B = 0.7 + 2 = 2.7$ For Silicon Transistor $V_{BE} = 0.7$

From equation (1)

$2.7/10 = R_2 / (R_1 + R_2)$ ----------(2)

$S = 1 + (R_B / R_E)$ $(S = 10)$

⇨ **$R_B = 9$ KΩ**

$R_B = R_1 R_2 / (R_1 R_2)$ ----------(3)

Substituting (2) in (3)

$9K\Omega = R_1 (0.27)$

$R_1 = 33$ KΩ **$R_2 = 12K\Omega$** **$C_E = 33\mu F$**

Feedback network

Let $L_1 = 0.1$mH $L_2 = 0.1$mH $C = 0.001\mu F$ $M = 20\mu H$

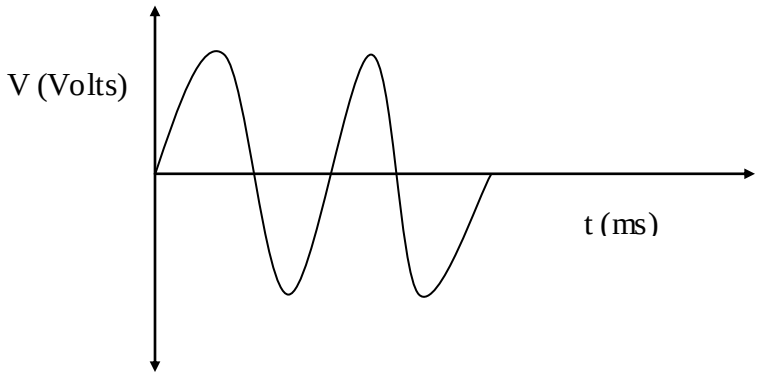
Operating frequency $f = \{ 1 / (2\pi\sqrt{L_T C}) \}$

$L_T = L_1 + L_2 + 2M$

⇨ $L_T = 2.4 \times 10^{-4}$ H

⇨ **f = 325 KHz.**

MODEL GRAPH



PROCEDURE

1. Connections are made as per the Given circuit diagram
2. Collector voltage signal is monitored in the CRO.
3. The frequency is calculated from the waveform obtained.
4. The graphs are plotted for V_{CE} Vs Time

APPLICATION

1. Hartley oscillator is very popular and is commonly used as a local oscillator in radio receivers.
2. It has two main advantages: Adaptability to wide range of frequencies and easy to tune.

REVIEW QUESTIONS:

1. What are the applications of LC oscillations?
2. What are the elements used in feedback network?
3. What is the expression for frequency of oscillations?
4. What is the difference between amplifier and oscillator?
5. What is the condition for oscillations?

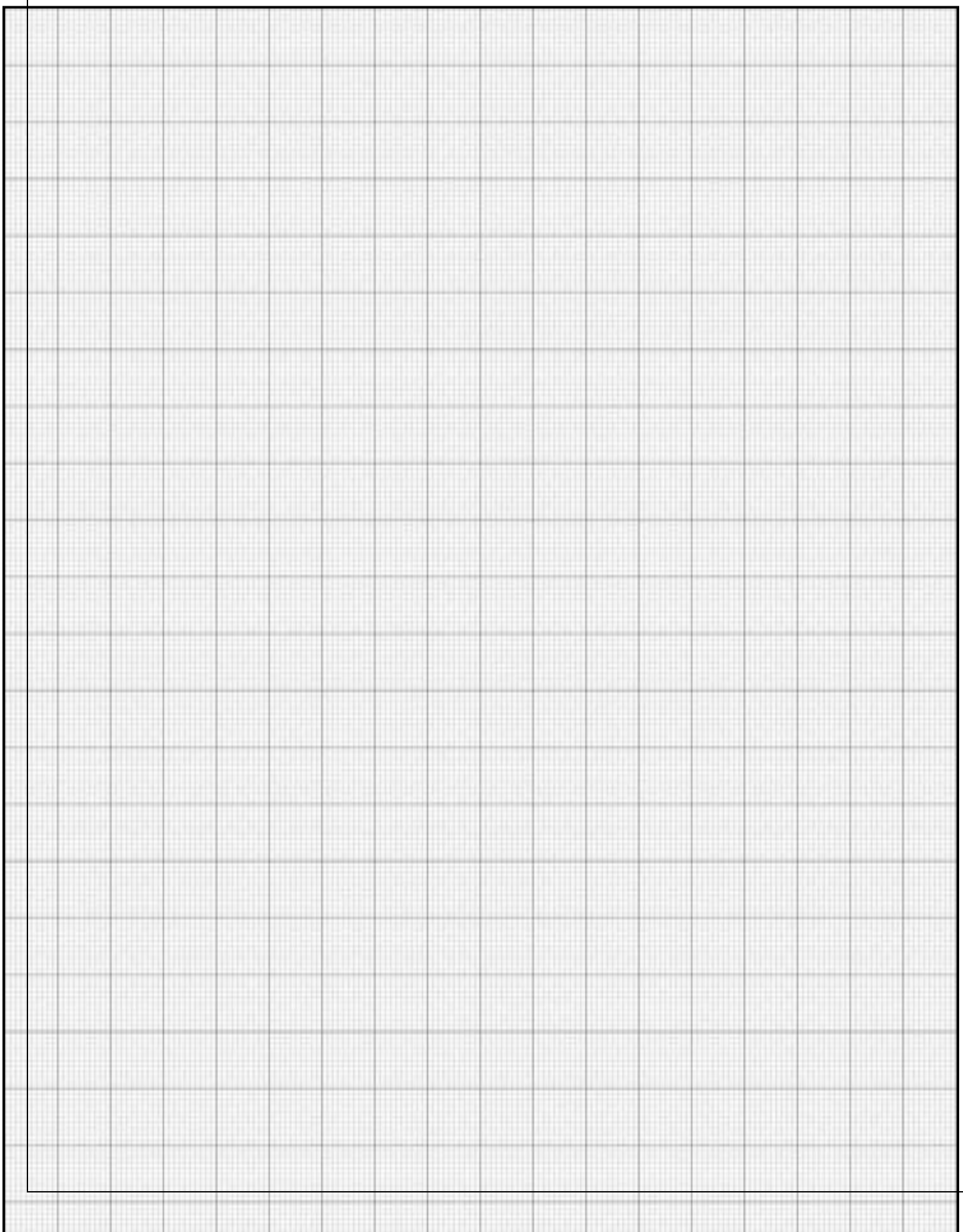
TABULATION

PARAMETER	COLLECTOR to EMITTER VOLTAGE (V_{CE}) in VOLTS
Amplitude	
Time Period	

MODEL CALCULATION

T =

f = 1 / T



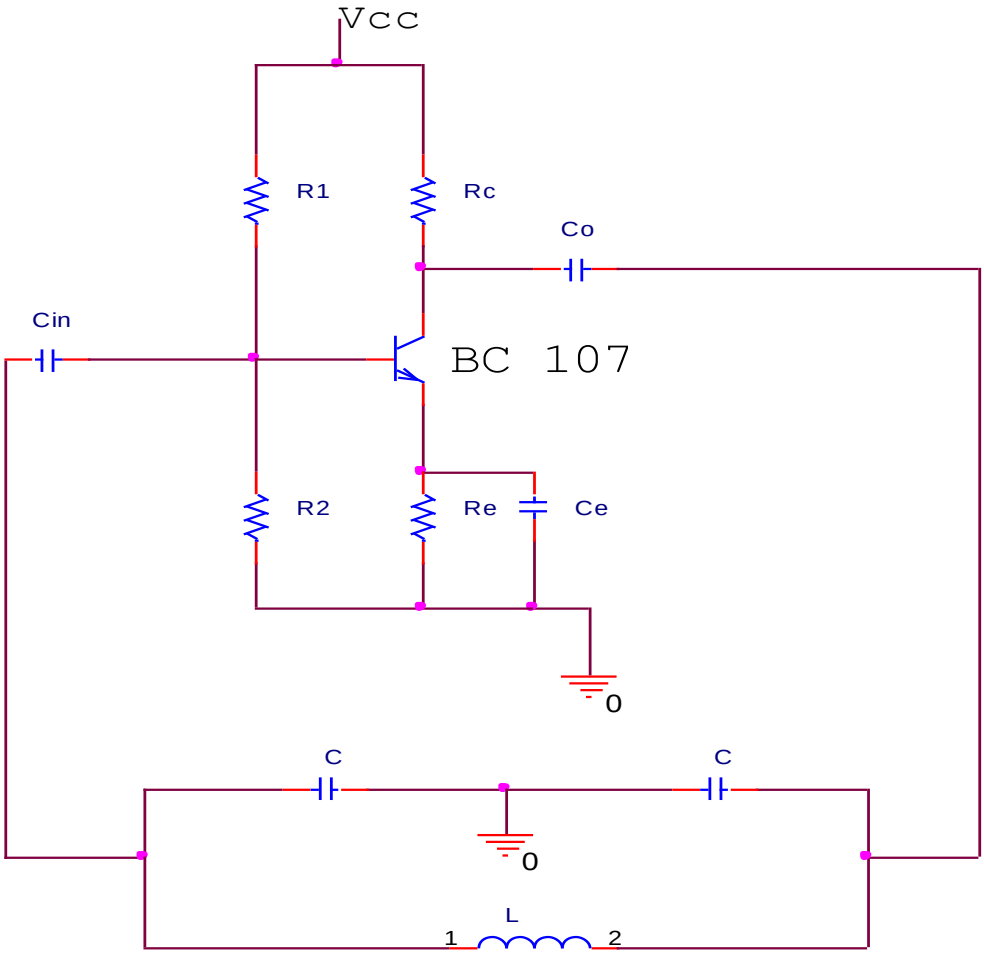
RESULT

Thus the Hartley oscillator is designed and oscillation is obtained

OSCILLATOR	DESIGN FREQUENCY	PRACTICAL FREQUENCY

MARKS ALLOCATION		
Experimental Setup	10	
Execution	10	
Viva	10	
Total	30	

COLPITTS OSCILLATOR



Ex. No:
Date:

COLPITTS OSCILLATOR

AIM

To design a Colpitt's oscillator to generate sinusoidal signal with a frequency of 225 KHz.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2	Transistor	BC 107	1
3	Resistor		
4	Capacitor		
5	Bread board	-	1
6	Power supply	(0-30)V	1
7	Decade inductance box		1
8	Decade capacitance box		1

THEORY

Colpitt oscillator circuit is widely used in commercial signal generators up to 100MHz.It basically consists of a single stage inverting amplifier and an LC phase shift network .The two series capacitors C_1 and C_2 form the potential divider used for providing the feedback voltage-the voltage developed across capacitor C_2 provides the regenerative feedback required for sustained oscillations. Parallel combination of R_E and C_E along with the resistors R_1 and R_2 provides the stabilized self bias.

The output of the phase shift LC network is coupled from the junction of L and C_2 to the amplifier input at base through coupling capacitor C_C, which blocks DC but provides path to AC.Transistor itself produces a phase shift of 180° and another phase shift of 180° is provided by the capacitive feedback. Thus a total phase shift of 360° is obtained which is the essential condition for developing oscillations. When the collector supply voltage V_{CC} is switched ON, the capacitor C_1 and C_2 are charged. These capacitors C_1 and C_2 discharge through the coil L, setting up oscillations of frequency : $f = 1/ 2\pi \sqrt{(1/ LC_1 + 1/ LC_2)}$

DESIGN

Biasing Network

$V_{CE} < V_{CC} / 2$

$V_{CE} < 10 / 2$

⇨ $V_{CE} = 4V$

Kirchoff's Voltage law for output circuit:

$V_{CC} - V_{CE} = I_C R_C + I_E R_E$ $\quad I_C \approx I_E = 2$ mA

⇨ $10 – 4 - I_C(R_C + R_E) = 0$

⇨ $R_C + R_E = 6 \times 10^3 / 2$

⇨ **$R_E = 1$ KΩ**

To find R_1 and R_2

$V_B = V_{CC} R_2 /(R_1 + R_2)$ ---------- (1)

Also $V_B = V_{BE} + V_E$

$V_B = 0.7 + 2 = 2.7$ For Silicon Transistor $V_{BE} = 0.7$

From equation (1)

$2.7/10 = R_2 /(R_1 + R_2)$ ---------- (2)

$S = 1 + (R_B / R_E)$ $(S = 10)$

⇨ **$R_B = 9$ KΩ**

$R_B = R_1 R_2 / (R_1 R_2)$ ---------- (3)

Substituting (2) in (3)

$9 = R_1 (0.27)$

$R_1 = 33$ KΩ **$R_2 = 12$KΩ** **$C_E = 33$μF**

Feedback network Design

Let

$C_1 = 0.01$μF $C_2 = 0.01$μF L = 0.1mH

Operating frequency $f = \{ 1/(2\pi\sqrt{C_T L}) \}$

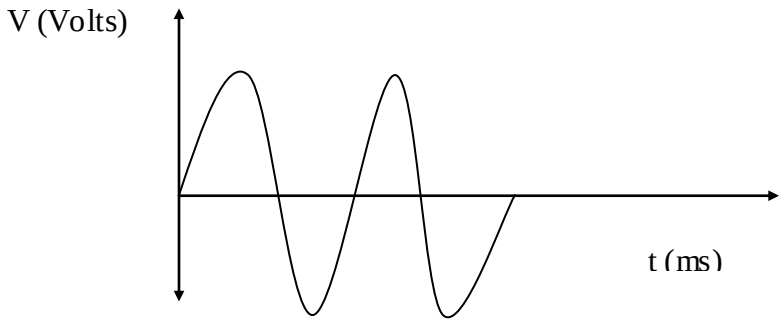
$C_T = C_1 C_2 /(C_1 + C_2)$

⇨ $C_T = 0.005$μF

⇨ **f = 225 KHz.**

The oscillations across capacitor C_2 are applied to the base emitter junction and appear in the amplified form in the collector circuit. Of course, the amplified output in the collector circuit is of the same frequency as that of the oscillatory circuit. This amplified in the collector circuit is supplied to the tank circuit in order to meet the losses. Thus the tank circuit is getting continuous energy from the circuit to make up the losses occurring in it and therefore ensures undamped oscillations.

MODEL GRAPH



PROCEDURE

1. Connections are made as per given circuit diagram.
2. Connect CRO output terminals and observe the waveform.
3. Calculate practically the frequency of oscillations by using the expression

   f = 1 / T (T= Time period of the waveform)
4. Repeat the above steps 2, 3 for different values of L, and note down the practically values of oscillations of the colpitts oscillator.
5. Compare the values of oscillations both theoretically and practically.

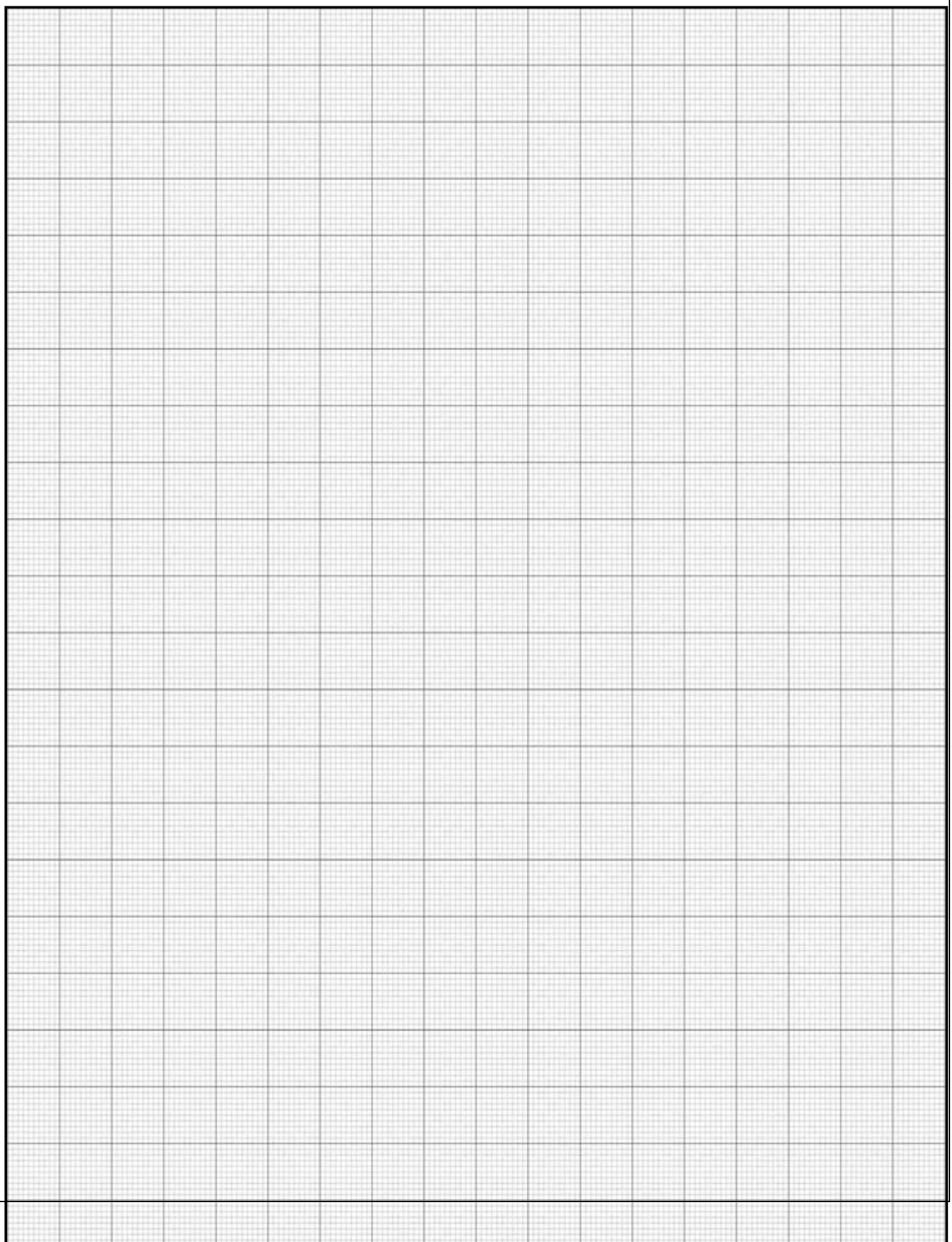
TABULATION

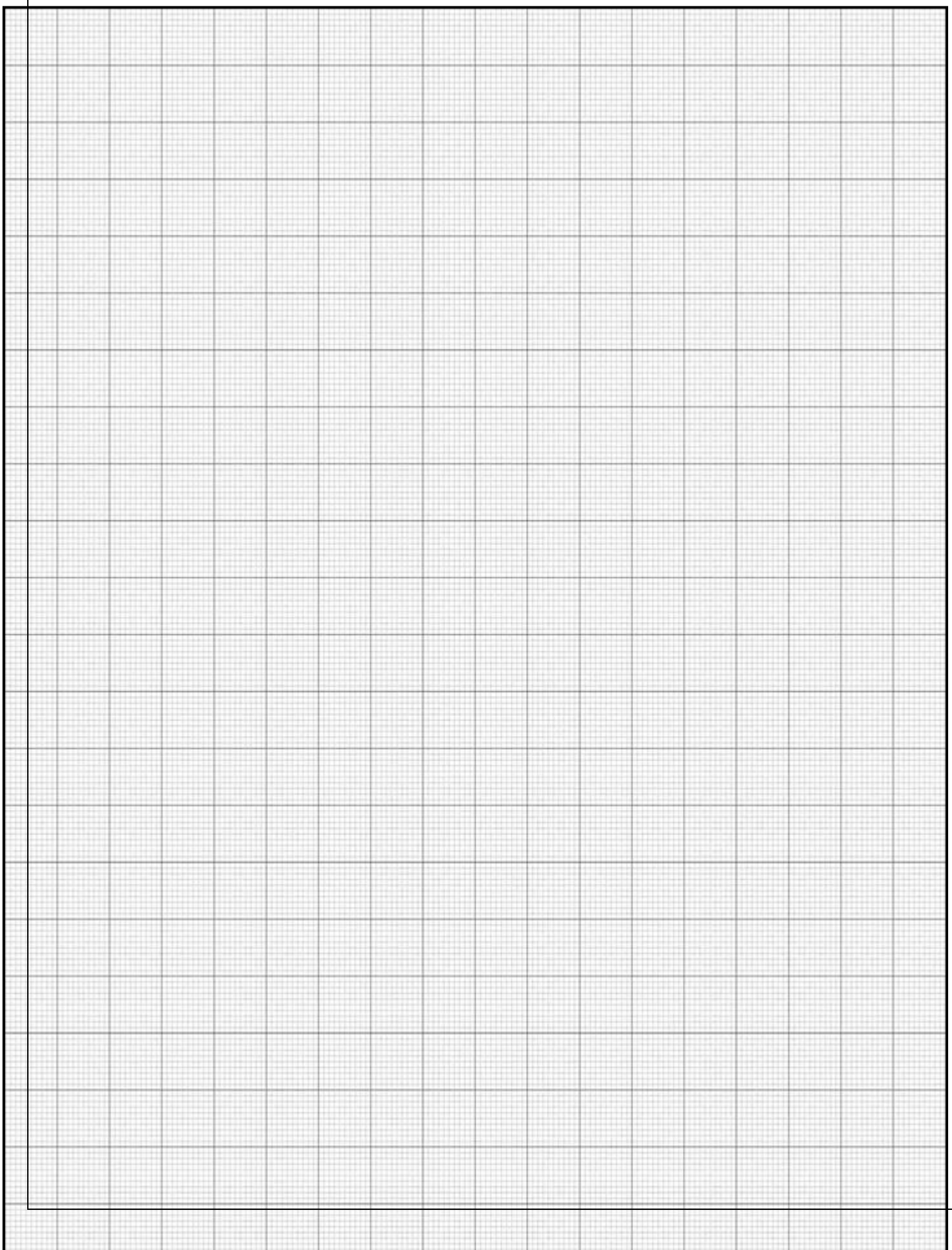
PARAMETER	COLLECTOR to EMITTER VOLTAGE (V_{CE}) in VOLTS
Amplitude	
Time Period	

MODEL CALCULATION

T =

f = 1 / T =





REVIEW QUESTIONS:

1. What are the applications of LC oscillators?
2. What type of feedback is used in oscillators?
3. What is the expression for the frequency of oscillations of colpitt's oscillator?
4. How does Colpitt's differ from Hartley?
5. What is the function of input and output capacitor?
6. What is the condition for sustained oscillations in this oscillator?

RESULT

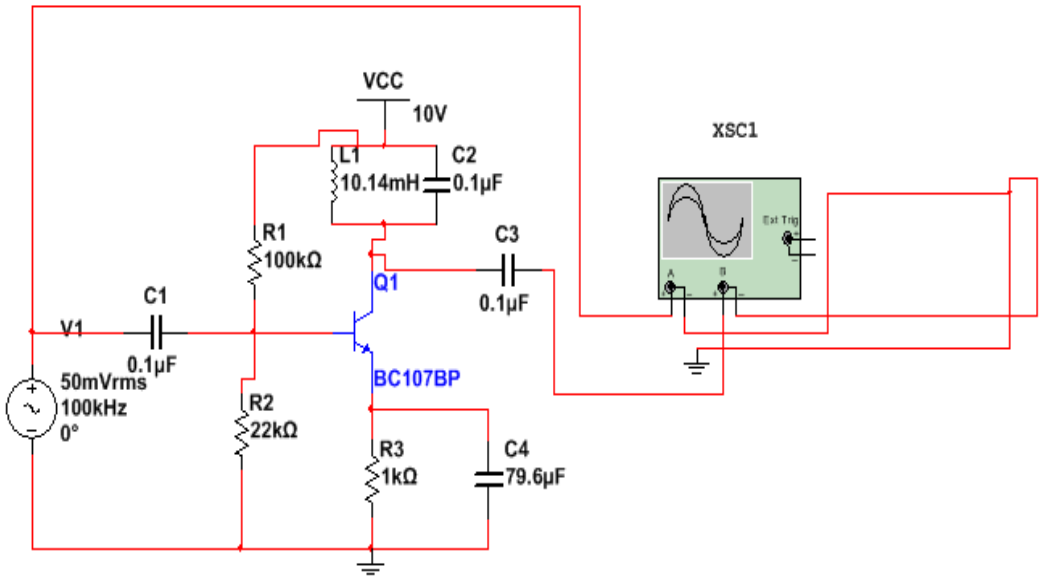
Thus the Colpitt's oscillator is designed and oscillation is obtained

OSCILLATOR	DESIGN FREQUENCY	PRACTICAL FREQUENCY

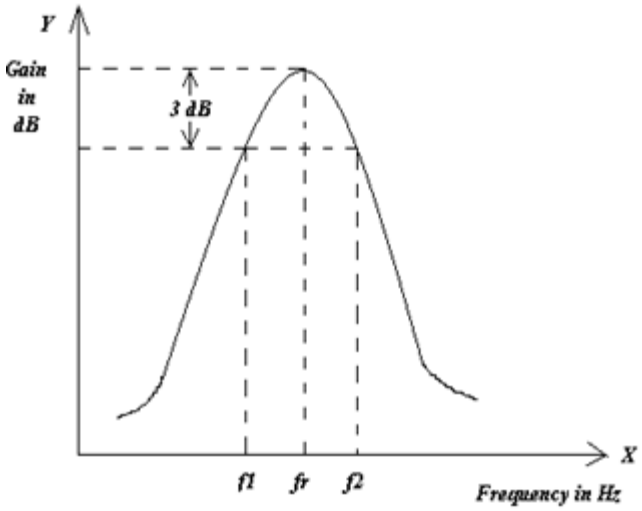
MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

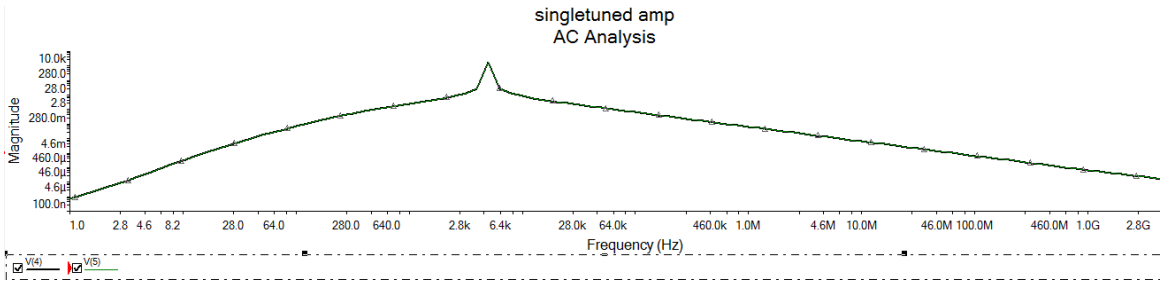
CIRCUIT DIAGRAM

SINGLE TUNED AMPLIFIER



MODEL GRAPH





Ex. No:
Date:

SINGLE TUNED AMPLIFIER

AIM

To design and construct the Single Tuned Amplifier for given resonant frequency *f*o= 3KHz Also obtain the frequency response of tuned amplifier and to find bandwidth and quality factor.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Function Generator	(0-2)MHz	1
3.	Transistor	BC 107	1
4.	Resistor		
5.	Capacitor		
6.	Bread board	-	1
7.	Power supply	(0-30)V	1

THEORY

The efficiency of output circuit of an amplifier increases as the operation is shifted from class-A to B and then to C. In class-C amplifiers efficiency approaches 100%. But the difficulty with class-C operation is harmonic distortion is more. It is tuned amplifier and only one frequency fo is to be amplified and power to be handled Po is large. Since efficiency is high and harmonic distortion will not be a problem since only one frequency is to be amplified and the tuned circuit will reject the other frequencies.

The functions of resonant circuits are:

1. To provide correct load impedance to the amplifier.
2. To reject unwanted harmonics.
3. To couple the power to load

The resonant circuits in tuned power amplifier are called tank circuits.

Formula

f0=1/ 2π√LC)

Quality factor = f0/BW

Bandwidth = fH – fL

f0 – Resonant frequency

fL – Lower cutoff frequency

fH – Upper cutoff frequency

DESIGN

Tank Circuit

f0 = 1/ (2π√LC)

Given f0 = 5 KHz, Assume C =0.1µF

L = 10.14 mH

Amplifier Design

Transistor BC 147

hfe min = 200, IC = 1mA

Assume VCC=10V

Selection of RE, R2 and R1

VRE = 1/10 x VCC = 1/10 x 10 = 1V

IE = IC = 1mA

RE =VRE/IE=1V/1mA= 1KΩ

Select RE=1KΩ

R2 = hfe min RE/10 = 20KΩ

Select R 2=22KΩ

13 VR1 =VCC - VR2

VR1 =VCC – (VBE - VRL)

VR1 =10 - (0.6+1) = 8.4V

VR1/VR2=R1/R2

R1= (VR1X R2)/ VR2 = 8.4 X 20K/1.6=105KΩ

Select

R1 =100KΩ

Coupling capacitor CC=0.1µF

Bypass capacitor CE

XCE =1/10 x RE =100Ω

XCE =1/(2πfCE)

Let f = 20Hz (lowest frequency of input signal)

CE=79.6µF

design for f0=3khz:

Quality factor = $\frac{Fo}{Bw}$

Bandwidth (Bw) = upper cutoff frequency – lower cut off frequency

PROCEDURE

1. Give the circuit as per circuit diagram
2. Set the input signal of amplitude 50 mV (pp) using signal generators
3. Apply the dc biasing voltage
4. Vary the input frequency and note down the output voltage
5. Draw the graph between frequencies and gain (dB)
6. *Calculate the gain and quality factor from graph*

REVIEW QUESTIONS:

1. What are the different types of tuned circuits?
2. How do you measure DC and AC power in the class C amplifier?
3. What is Q factor of a coil?
4. Calculate bandwidth of a Tuned amplifier whose resonant frequency is 15 KHz and Q-factor is 100.
5. What is the expression for efficiency of class-C tuned amplifier?
6. Specify the applications of Tuned amplifiers

TABULATION

V_{in}=

S.NO	FREQUNCY(Hz)	OUTPUT VOLTAGE (Vo)	GAIN (Vo/Vin)	GAIN IN dB (20 log (Vo/Vin)

RESULT

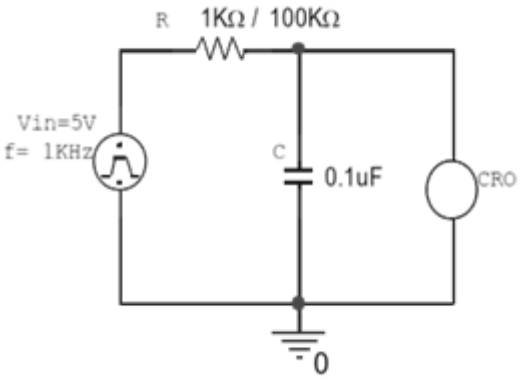
Thus the single tuned amplifier was designed for the given frequency and the following results are obtained.

S.NO	PARAMETER	VALUE
1	Mid band gain	
2	Upper cutoff frequency	
3	Lower cutoff frequency	
4	Bandwidth (F_H-F_L)	
5	Quality factor	

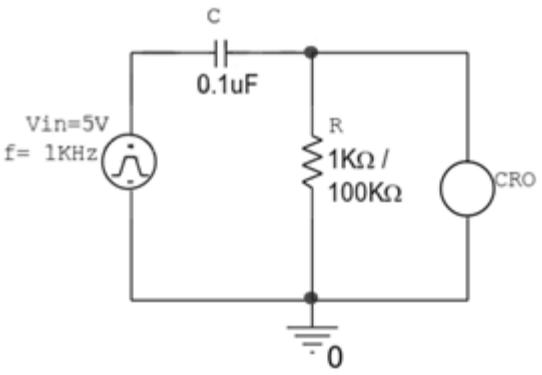
MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

CIRCUIT DIAGRAM

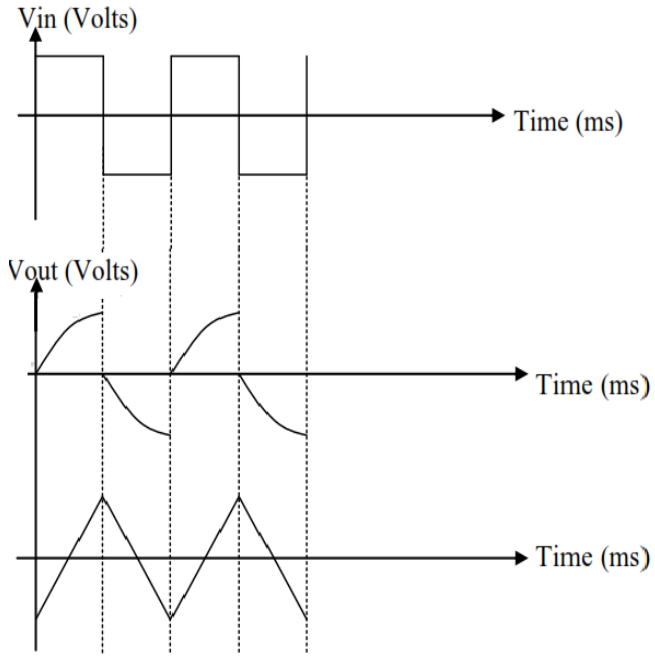
RC INTEGRATOR

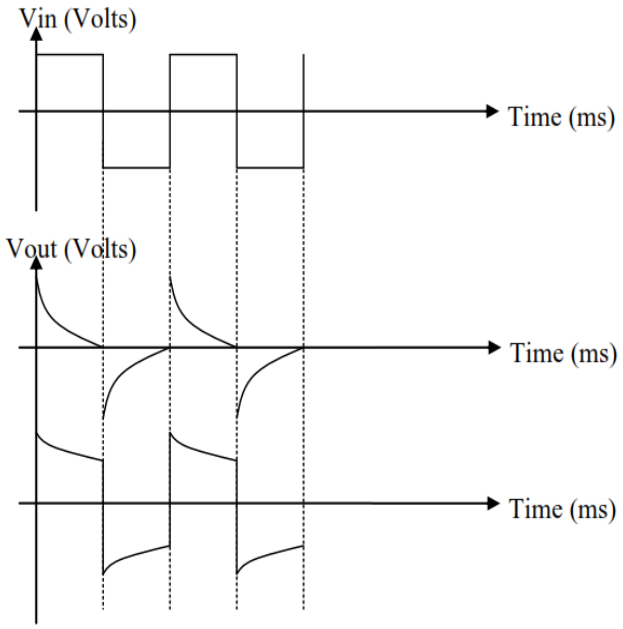


RC DIFFERENTIATOR



MODEL GRAPH





Ex. No:
Date:

RC INTEGRATOR & DIFFERENTIATOR CIRCUITS

AIM

To design and construct differentiator and integrator circuit by using passive element. Obtain the waveform for following input signal.

(i) Square waveform
(ii) Triangular waveform

APPARATUS AND EQUIPMENT REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Function Generator	(0-1)MHz	1
3.	Resistor		
4.	Capacitor		
5.	Bread board		1

THEORY

Differentiator:

The circuits, which make use of only linear circuit elements such as the inductors, capacitors and resistors, are known as linear wave shaping circuits. such circuits are used to perform function of differentiation and integration.

Differentiator is a circuit that passes high frequencies of the input and attenuates Low frequencies. It implies that the output voltage is the differential of the input.

$$v_o = RC\frac{dv_i}{dt}$$

A circuit in which the ouput voltage is directly proportional to the derivative of the input voltage is called as differentiating circuit.

Mathematically,

V α dVi/dt
= k. dVi/dt Where k is a constant

DESIGN

Integrator

f = 1 KHz

τ = RC = 1ms

If C = 0.1μF

Then R=10KΩ

For T << τ, Choose R = 1KΩ and

For T >> τ, Choose R = 100KΩ

Differentiator

f = 1 KHz

τ = RC = 1ms If C = 0.1μF

Then R=10KΩ

For T << τ, Choose R = 1KΩ and

For T >> τ, Choose R = 100KΩ

Application:

a. To generate a series of narrow pulses from rectangular or square waveforms. This used as a triggering pulses or synchronization pulses in television and CRO
b. To generate a step from a ramp input
c. To generate a square waveform from a triangular wave input.

Integrator:

Integrator is a circuit that passes low frequencies of the input and attenuates high frequencies. Integrator implies that the output voltage is an integral of the input voltage.

$$v_0 = \frac{1}{RC}\int v_i dt$$

Application:

a. To perform mathematical integration in analog computers
b. To generate a triangular wave from a square wave
c. To generate a saw tooth wave from a rectangular wave.

PROCEDURE

Integrator:

1. The connections are given as per the Given circuit diagram
2. Switch on the power supply, function generator and CRO.
3. Give square wave input to Integrator circuit and observe the output waveform in CRO. Note down the parameters amplitude and Time period.
4. Give Triangular wave input to Integrator circuit and observe the output waveform in CRO. Note down the parameters like amplitude and Time period
5. Draw the graph between time period and Amplitude.

Differentiator:

1. The connections are given as per the given circuit diagram
2. Switch on the power supply, function generator and CRO.
3. Give square wave input to differentiator circuit and observe the output waveform in CRO. Note down the parameters amplitude and Time period.
4. Give Triangular wave input to differentiator circuit and observe the output waveform in CRO. Note down the parameters like amplitude and Time period
5. Draw the graph between time period and Amplitude.

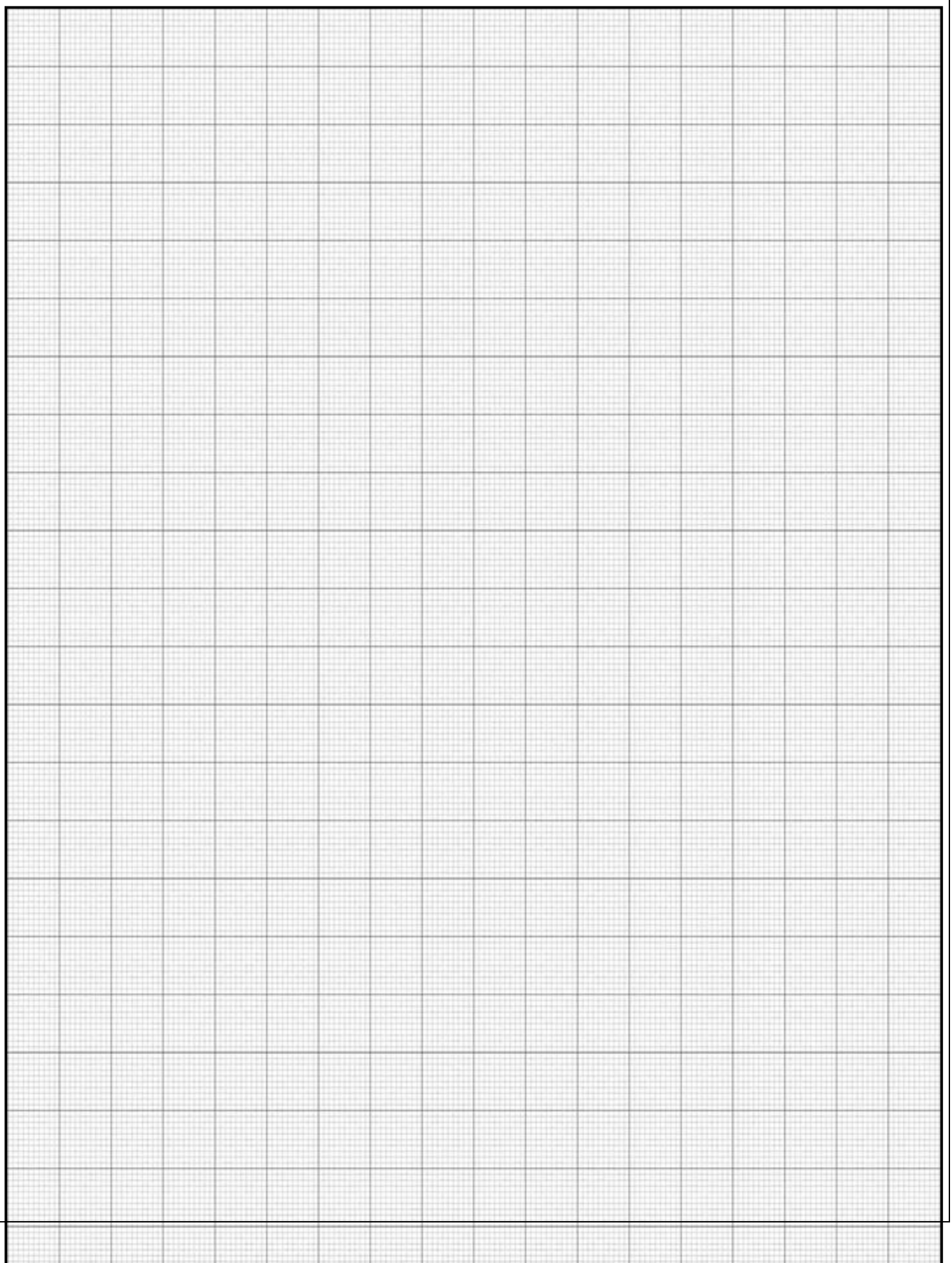
TABULATION

INTEGRATOR

Input Square Wave (V_{in} =)	Output Waveform	
	Amplitude	**Time period**
R=1K		
R=100k		

DIFFERENTIATOR

Input Square Wave (V_{in} =)	Output Waveform	
	Amplitude	**Time period**
R=1K		
R=100k		



REVIEW QUESTIONS:

1. Define differentiator & Define integrator
2. What are the limitations of an ordinary differentiator?
3. Explain how the practical differentiator will overcome the limitations
4. What are the limitations of an ideal integrator?
5. What are the initial conditions of a loss integrator?
6. What are the differences between integrator and differentiator?
7. State the applications of integrator & differentiator
8. Explain why integrators are preferred over differentiators in analog computer.

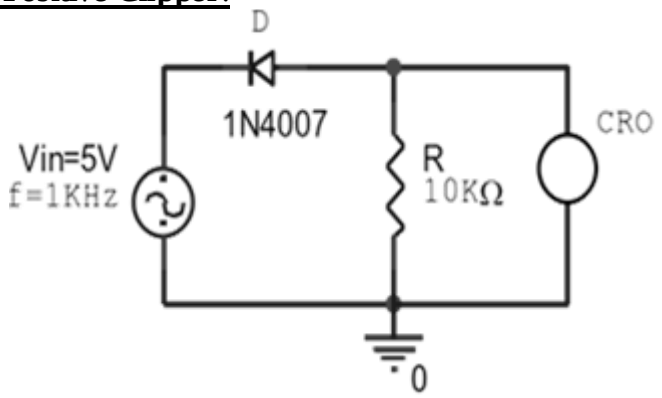
RESULT

Thus the RC integrator and differentiator circuits are designed and verified.

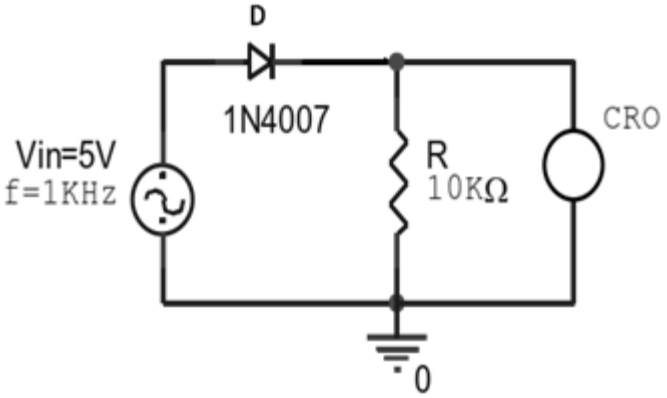
MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

CIRCUIT DIAGRAM

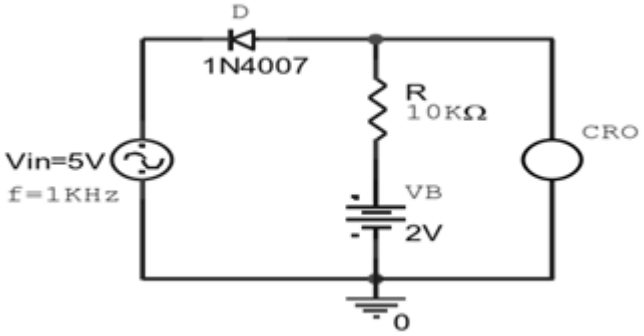
Series Positive Clipper:



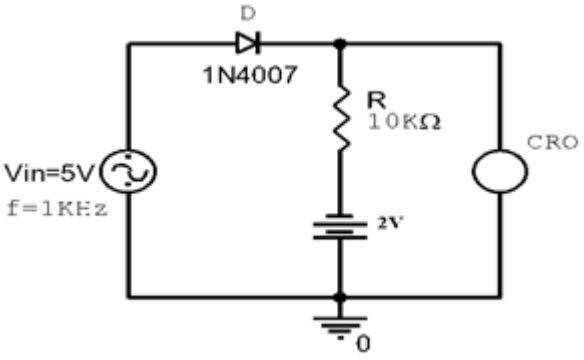
Series Negative Clipper:



Biased Series positive Clipper



Biased Series Negative Clipper:



Ex. No:
Date:

CLIPPERS AND CLAMPERS

AIM:

To design and construct the following clipper and clamper circuits and obtain the output waveform for the input sine wave signal.

a. Series clipper
b. Combinational clipper
c. Clamping circuit

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Function Generator	(0-2)MHz	1
3.	Power supply	(0-30)V	1
4.	Resistor		
5.	Capacitor		
6	Bread board	-	1
7	Diode	1N4007	2

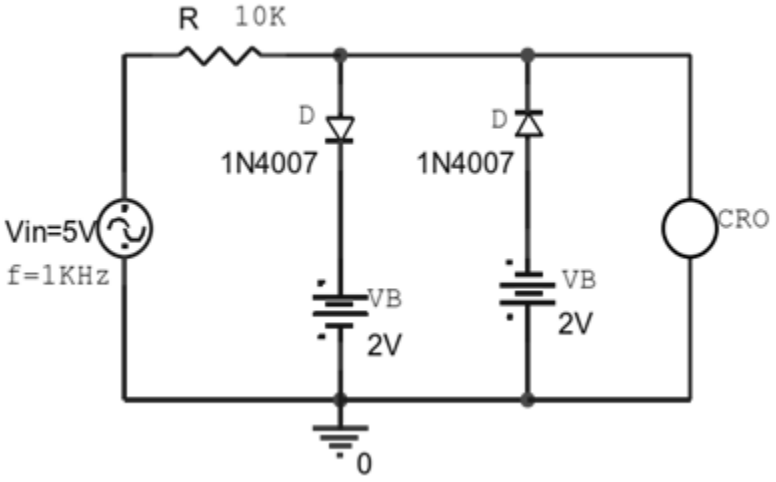
THEORY

Clipper:

The circuit which the wave form is shaped by removing or clipping a portion of the applied wave is known as clipping circuit. The important diode clippers are

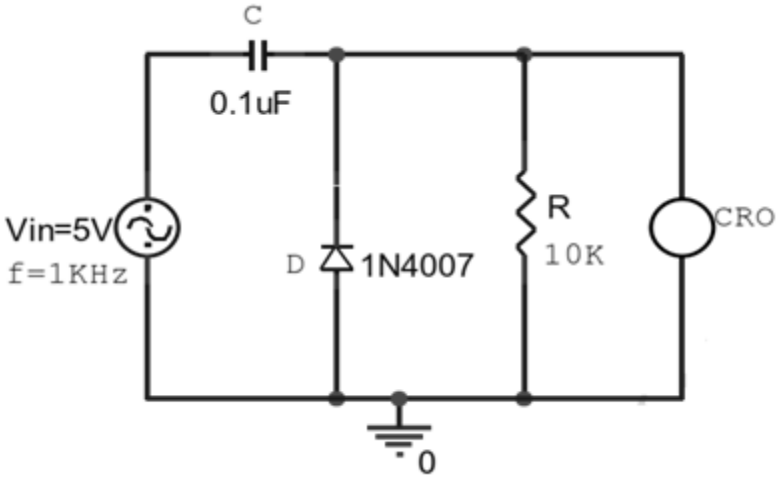
- Series clipper - Diode will be in series with output
  - Series Positive clipper
  - Series biased Positive clipper
  - Series Negative clipper
  - Series biased Negative clipper
- Combinational clipper
  - It is a combination of positive and negative clipper

Combinational Clipper

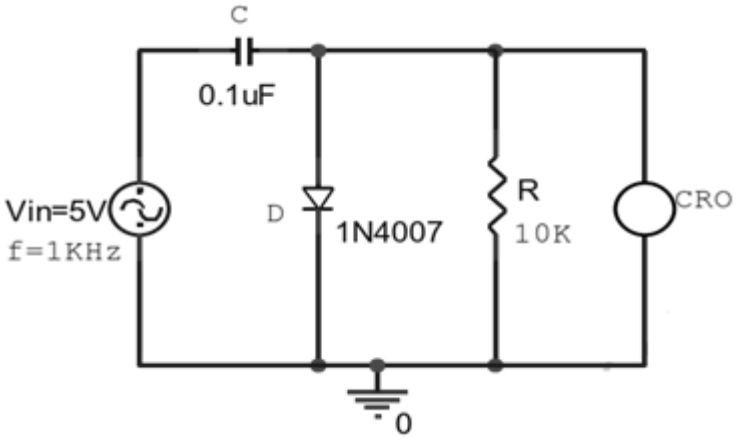


CLAMPER CIRCUIT

Positive Clamper



Negative Clamper



In a SERIES LIMITER or SERIES CLIPPER, a diode is connected in series with the output. The input signal is applied across the diode and resistor and the output is taken across the resistor. The series-limiter circuit can limit either the positive or negative alternation, depending on the polarity of the diode connection with respect to ground.

Diode D1 is in series with the output and the output is taken across resistor R1. The input must be negative with respect to the anode of the diode to make the diode conduct. When the positive alternation of the input signal is applied to the circuit, the cathode is positive with respect to the anode. The diode is reverse biased and will not conduct. Since no current can flow, no output is developed across the resistor during the positive alternation of the input signal.

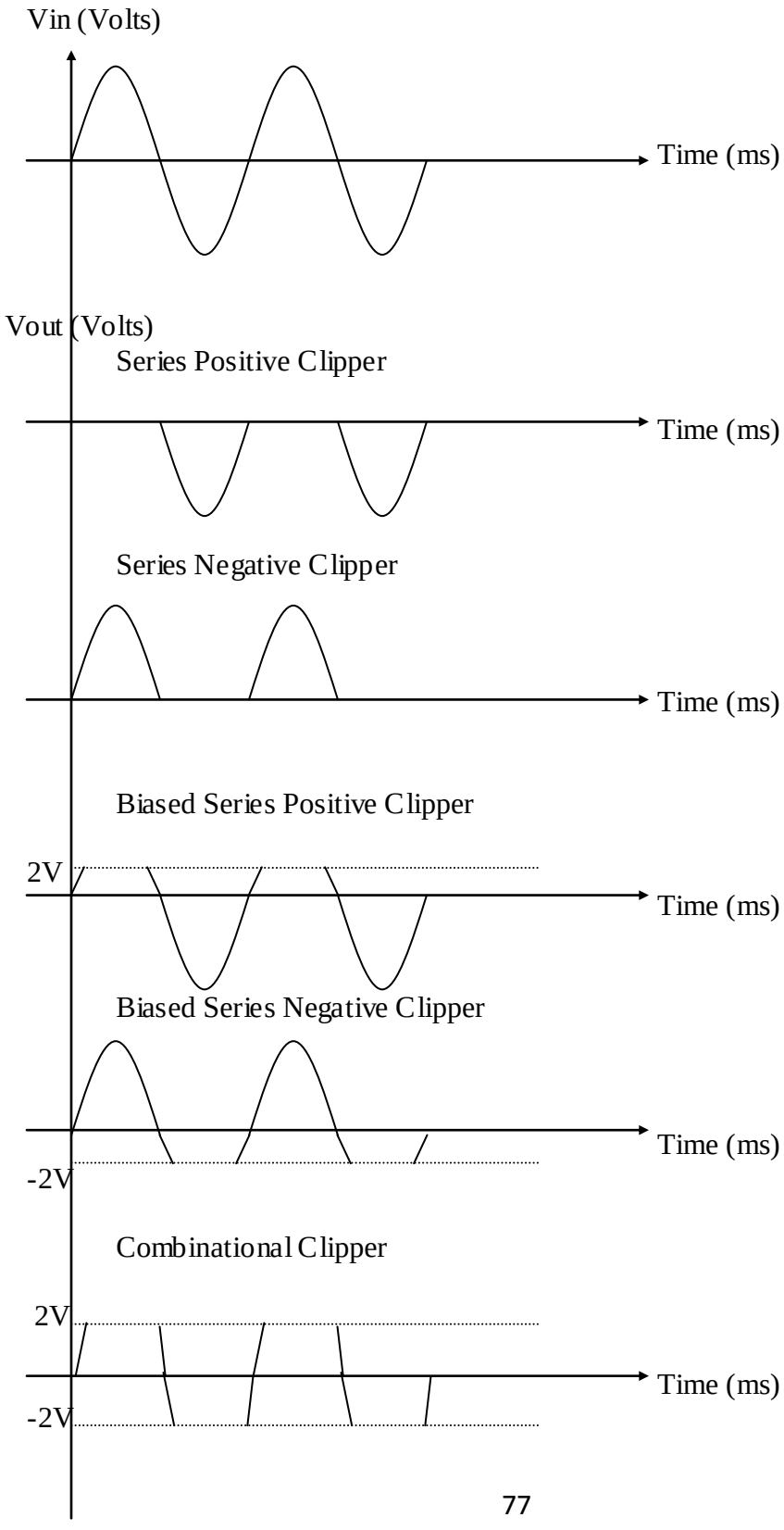
During the negative half cycle of the input signal, the cathode is negative with respect to the anode. This causes D1 to be forward biased. Current flows through R1 and an output is developed .The output during each negative alternation of the input is approximately the same as the input because most of the voltage is developed across the resistor.

CLAMPERS

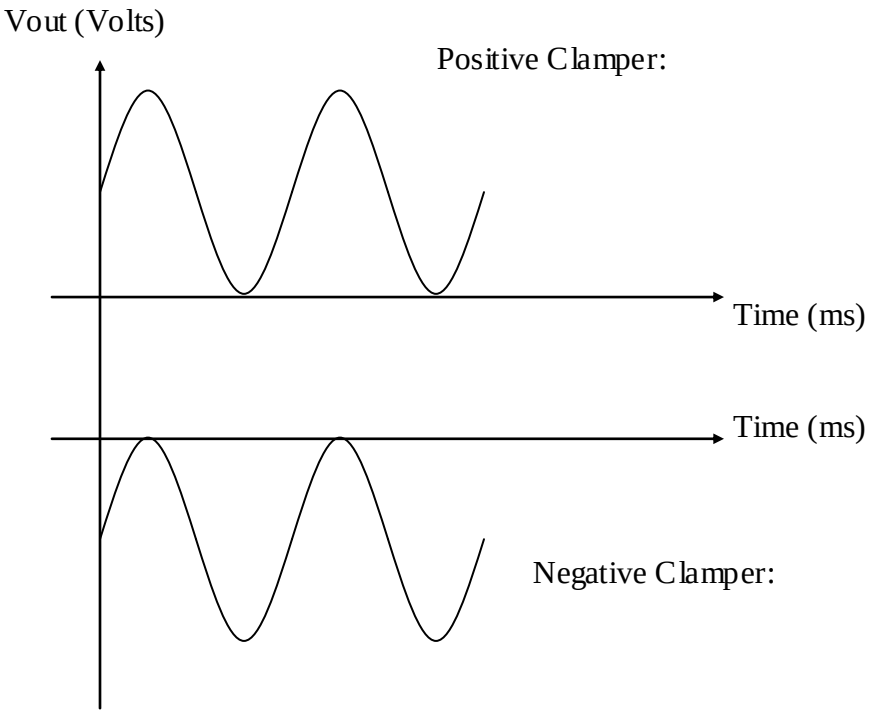
Certain applications in electronics require that the upper or lower extremity of a wave be fixed at a specific value. In such applications, a CLAMPING (or CLAMPER) circuit is used. A clamping circuit clamps or restrains either the upper or lower extremity of a waveform to a fixed dc potential. This circuit is also known as a DIRECT-CURRENT RESTORER or a BASE-LINE STABILIZER. Such circuits are used in test equipment, radar systems, electronic countermeasure systems, and sonar systems. Depending upon the equipment, you could find negative or positive clampers with or without bias.

MODEL GRAPH

CLIPPER:



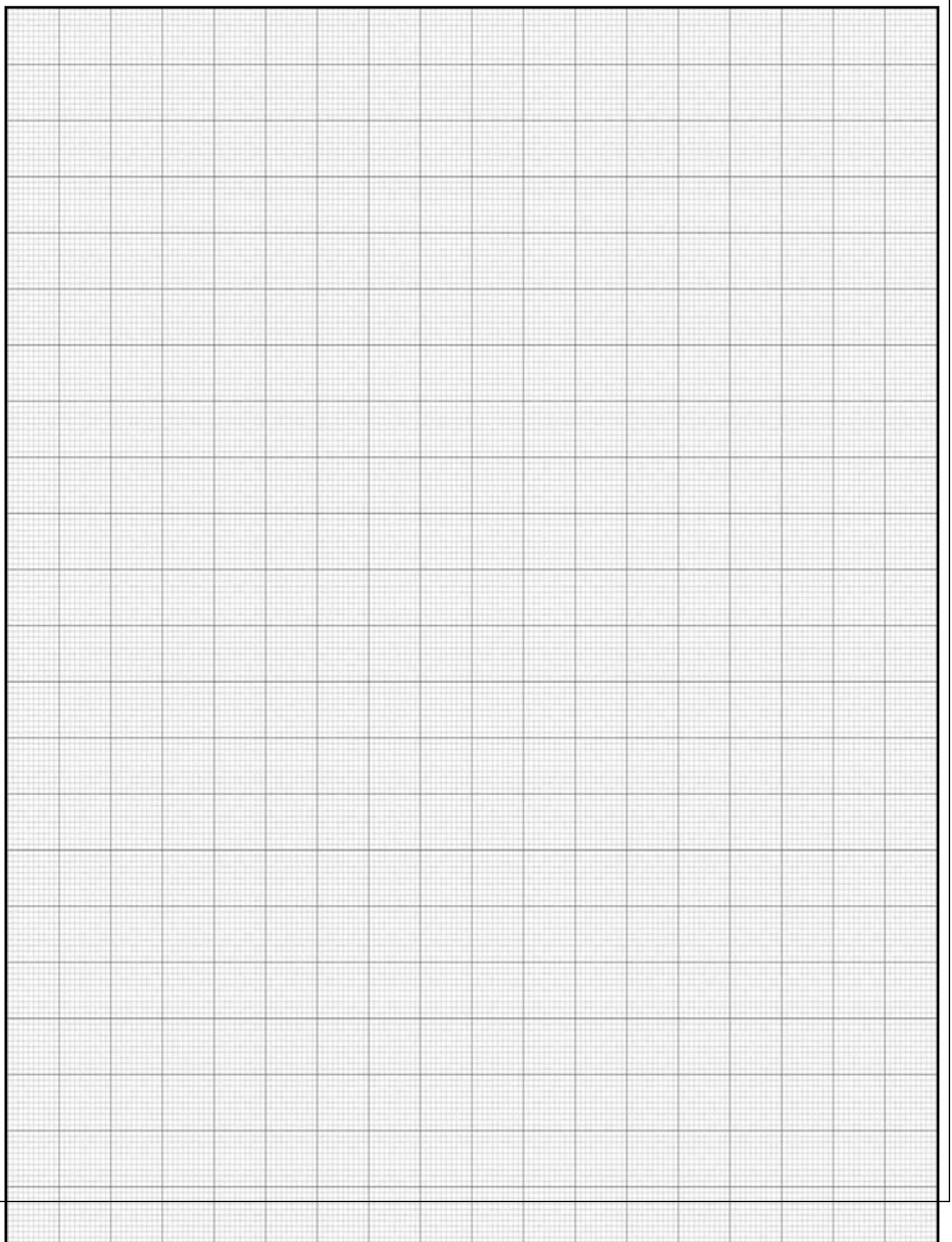
CLAMPER OUTPUT

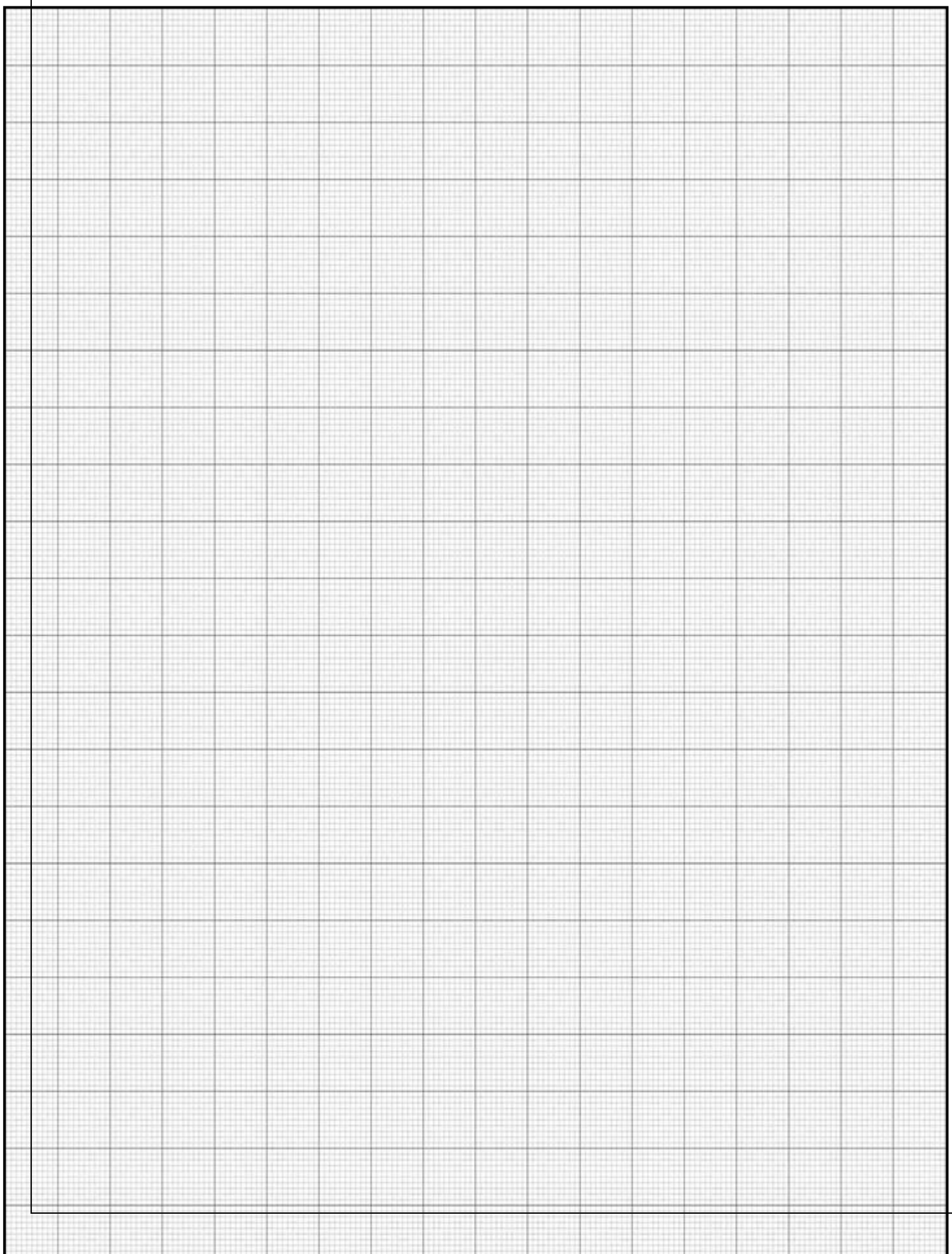


TABULATION:

Input Signal (Vin)=_____

S.no	Clipper and clamper circuits	Amplitude in volts	Time period in ms
1.	Series Positive Clipper		
2.	Series Negative Clipper		
3.	Biased Series Positive Clipper		
4.	Biased Series Negative Clipper		
5.	Combinational Clipper		
6.	Positive Clamper:		
7.	Negative Clamper:		





REVIEW QUESTIONS:

1. Define clamper and clipper?
2. Define series and shunt clipper?
3. Draw the series negative clipper circuit?
4. Mention application of clipper?
5. Mention application of clamper?

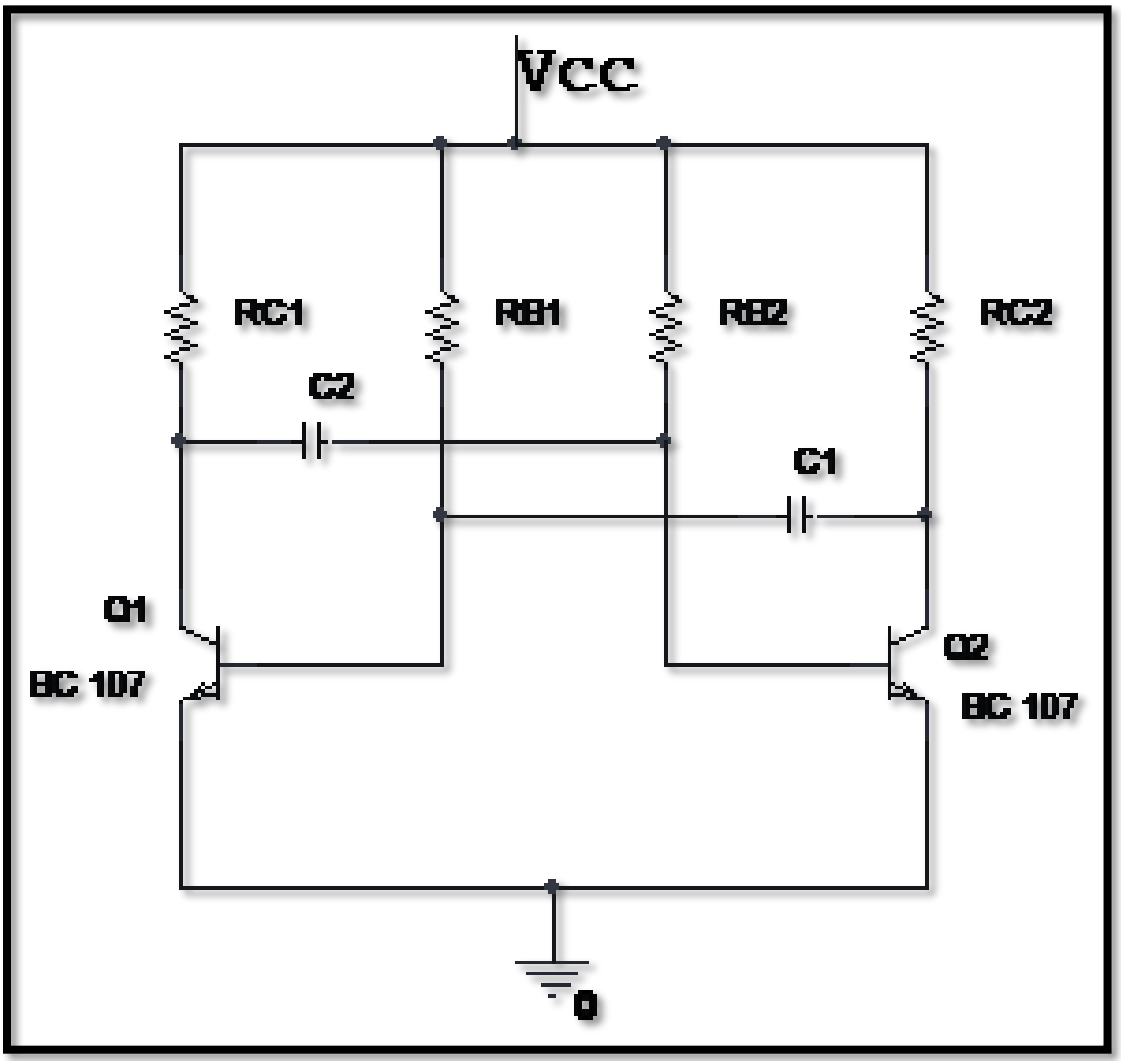
RESULT

Thus the different types of clipper and clamper circuits are constructed and outputs are noted

MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

CIRCUIT DIAGRAM

ASTABLE MULTIVIBRATOR



Ex. No:
Date:

ASTABLE MULTIVIBRATOR

AIM

To design collector coupled astable multivibrator to generate 3 KHz square wave.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1	CRO	(0-30) MHz	1
2	Transistor	BC 107	2
3	Resistor		
4	Capacitor		
5	Bread board	-	1
6	Power supply	(0-30)V	1

THEORY

The type of circuit most often used to generate square or rectangular waves is the multivibrator. A multivibrator, as shown in figure, is basically two amplifier circuits arranged with regenerative feedback. One of the amplifiers is conducting while the other is cut off.

When an input signal to one amplifier is large enough, the transistor can be driven into cutoff, and its collector voltage will be almost V_{CC}. However, when the transistor is driven into saturation, its collector voltage will be about 0 volts. A circuit that is designed to go quickly from cutoff to saturation will produce a square or rectangular wave at its output. This principle is used in multivibrators. Multivibrators are classified according to the number of steady (stable) states of the circuit. A steady state exists when circuit operation is essentially constant; that is, one transistor remains in conduction and the other remains cut off until an external signal is applied.

The three types of multivibrators are the

- ASTABLE,
- MONOSTABLE
- BISTABLE.

DESIGN

V_{CC} = 12 V: I_C= 5 mA; $h_{FE\ (MIN)}$ = 100; $V_{CE(SAT)}$ = 0.2 V ; $I_{B(Sat)}$ = 50µA

R_{C1}= R_{C1}= (V_{CC}- $V_{CE(SAT)}$)/I_C

I_B = I_C/ $h_{FE\ (MIN)}$

R_{B1}=R_{B2}=R_B= (V_{CC}-V_{BE})/I_B

Total Time T = t_1+t_2 = 0.5 ms

Time period equation of astable multivibrator is

$$T = 0.69 (R_{B1}C_1+R_{B2}C_2)$$

Where R_{B1}=R_{B2}=R_B and C_1=C_2 = C

Therefore $T = 1.38\ R_B * C$

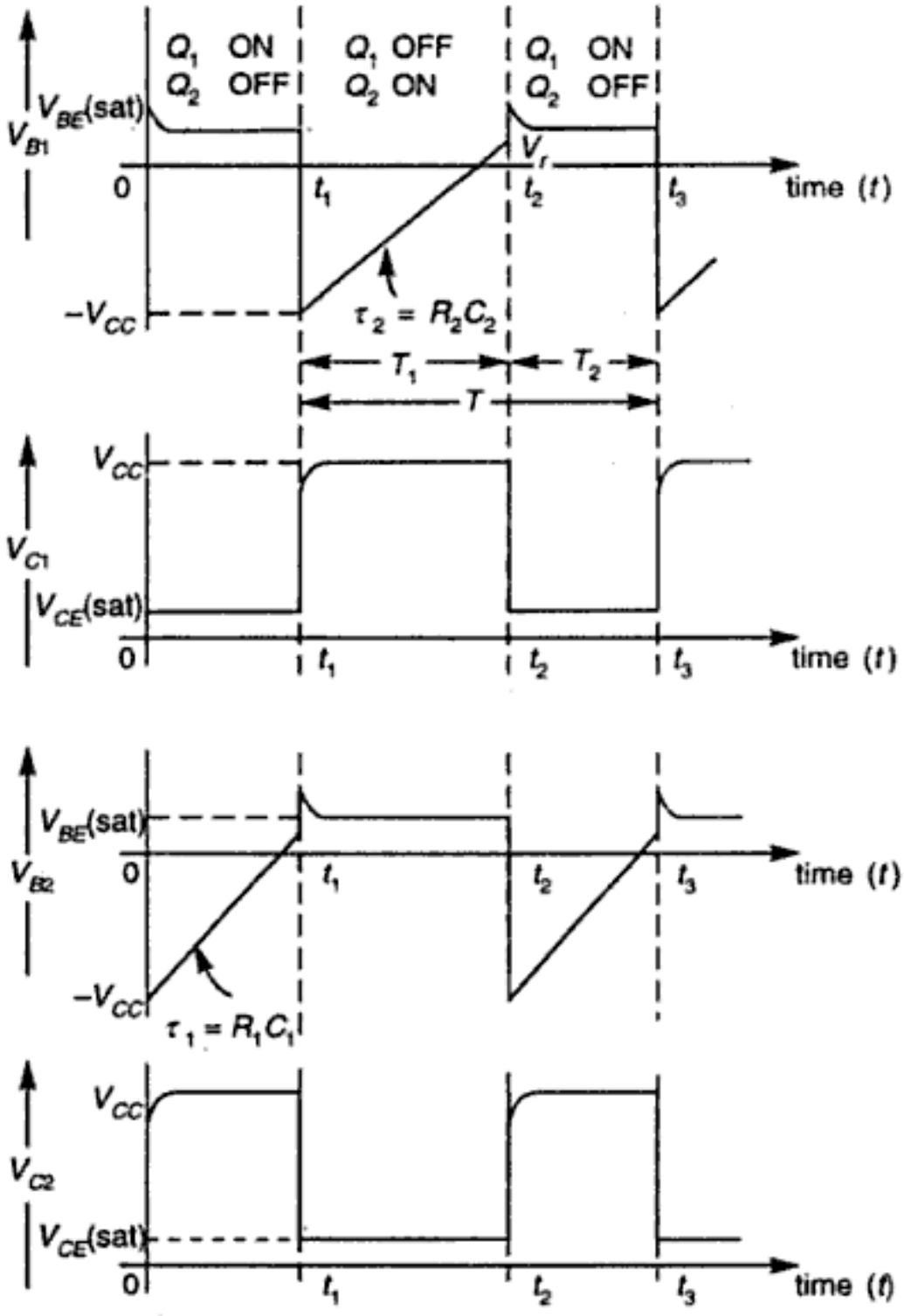
$C = T/ (1.38 * R_B)$

The astable circuit has no stable state. With no external signal applied, the transistors alternately switch from cutoff to saturation at a frequency determined by the RC time constants of the coupling circuits. An astable multivibrator is also known as a FREE-RUNNING MULTIVIBRATOR. It is called free- running because it alternates between two different output voltage levels during the time it is on. The output remains at each voltage level for a definite period of time. If you looked at this output on an oscilloscope, you would see continuous square or rectangular waveforms. The astable multivibrator has two outputs, but NO inputs

CONSTRUCTION:

- A multivibrator in which neither stage is at a stable state and the stages are switched from one state to another at regular time intervals without any triggering.
- Collector – coupled astable multivibrator consists of two identical NPN transistors *Q1* and *Q2*.
- It is possible to have $Rc_1 = Rc_2 = Rc$, $R_1 = R_2 = R$ and $C_1 = C_2 = C$. In the case, the circuit is known as symmetrical astable multivibrator.
- The transistor *Q1* is forward biased by the Vcc supply through resistor R_1. Similarly, the transistor *Q2* is forward biased by the Vcc supply through resistor R_2.
- The output of the transistor *Q1* is coupled to the input of transistor *Q2* through the capacitor C_1. Similarly, the output of transistor *Q2* is coupled to the input of transistor *Q1* through the capacitor C_2.
- Both transistors acts as switch and connected back to back each other.
- R_1C_1 and R_2C_2 forms the charging and discharging network i.e., time constant network.
- R_{C1} and R_{C2} acts as load resistors which is connected with biasing voltage V_{CC}.
- However, the two outputs are 180^o out of phase with each other. Therefore one of the output is said to be the complement of the other.

MODEL GRAPH


Q_1 ON
Q_2 OFF
Q_1 OFF
Q_2 ON
Q_1 ON
Q_2 OFF
V_{BE}(sat)
V_{B1}
V_r
0
t_1
t_2
t_3
time (t)
$-V_{CC}$
$\tau_2 = R_2C_2$
T_1
T_2
T
V_{CC}
V_{C1}
V_{CE}(sat)
V_{BE}(sat)
V_{B2}
$-V_{CC}$
$\tau_1 = R_1C_1$
V_{C2}
V_{CE}(sat)

PROCEDURE

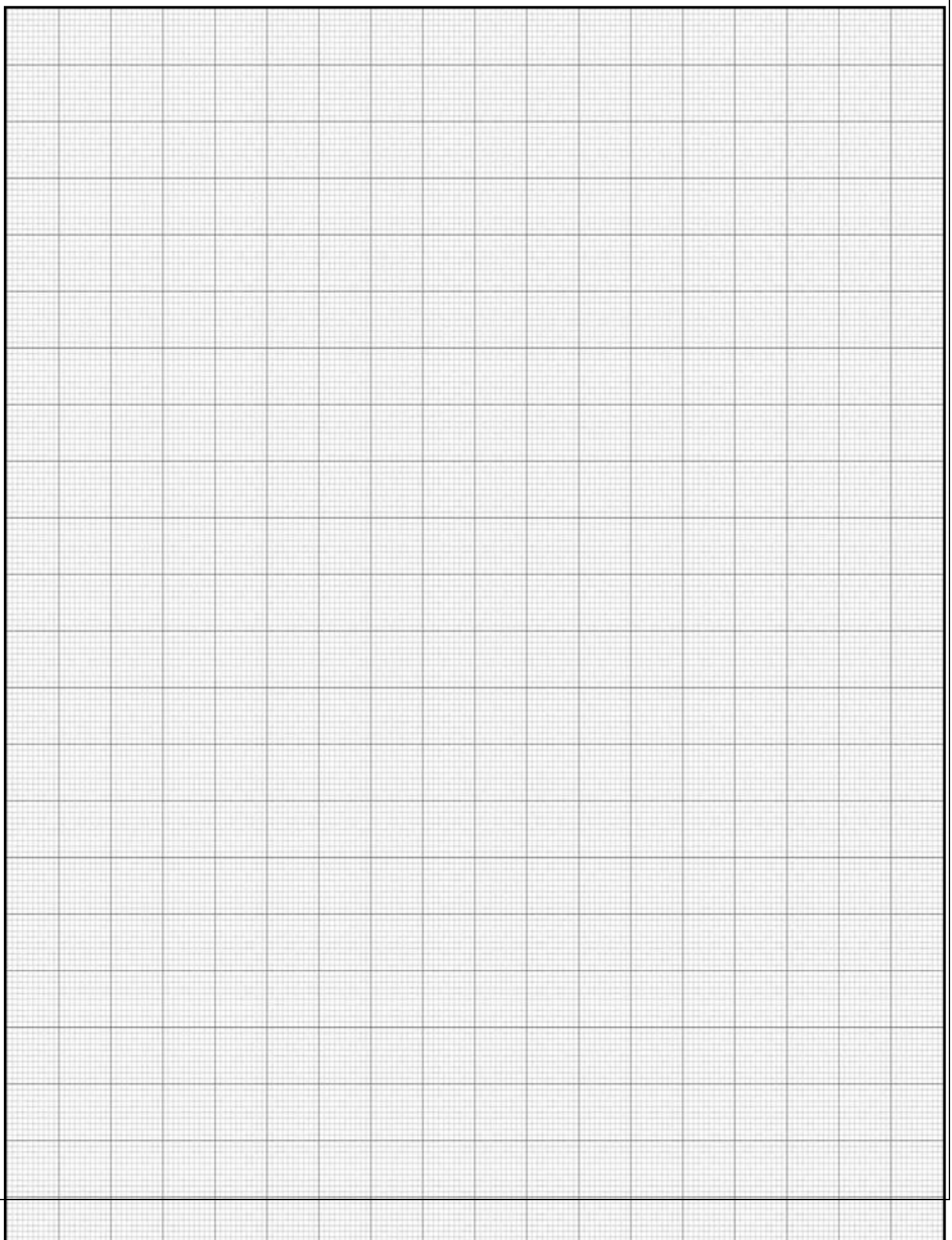
1. The circuit diagram is given as per given circuit diagram
2. The dc supply is switched ON
3. The collector terminal of transistor connected to CRO
4. The output voltage and time period are measured across transistors Q1 & Q2 at both the emitter and collector
5. The waveforms are plotted on a graph

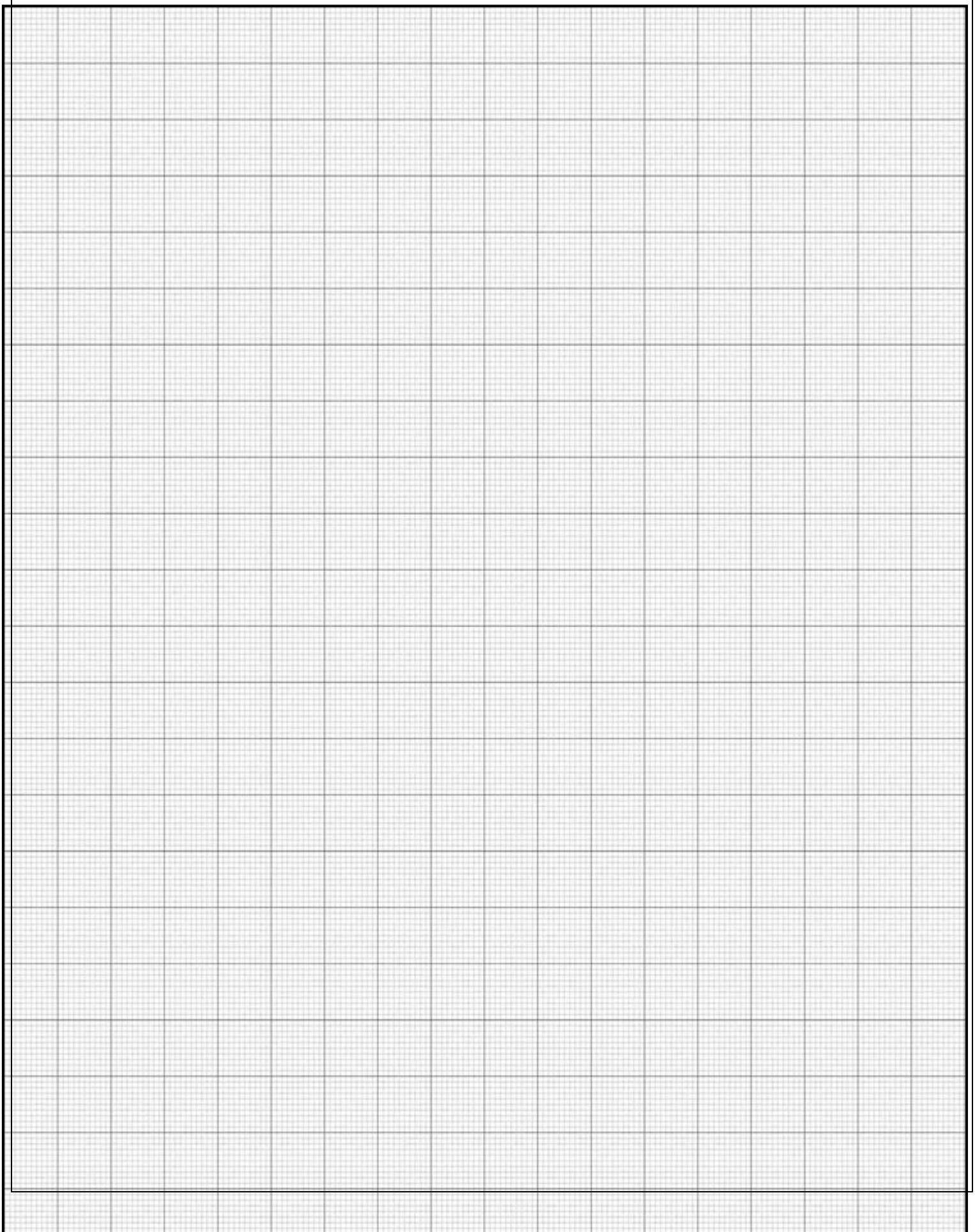
REVIEW QUESTIONS:

1. Define multivibrator?
2. What is the basic principle of multivibraotr?
3. Mention classification of multivibrator?
4. Why astable multivibrator is called as free running oscillator?
5. Mention Application of astable multivibrator?
6. Write time period equation of astable multivibrator?
7. Define duty cycle

OBSERVATION

S.No	Parameters	Across Q1	Across Q2
1	V_{BE}		
2	$-V_{CC}$		
3	V_{CC}		
4	$V_{CE(SAT)}$		
5	Time on		
6	Time off		
7	Total time		
8	Frequency		





RESULT

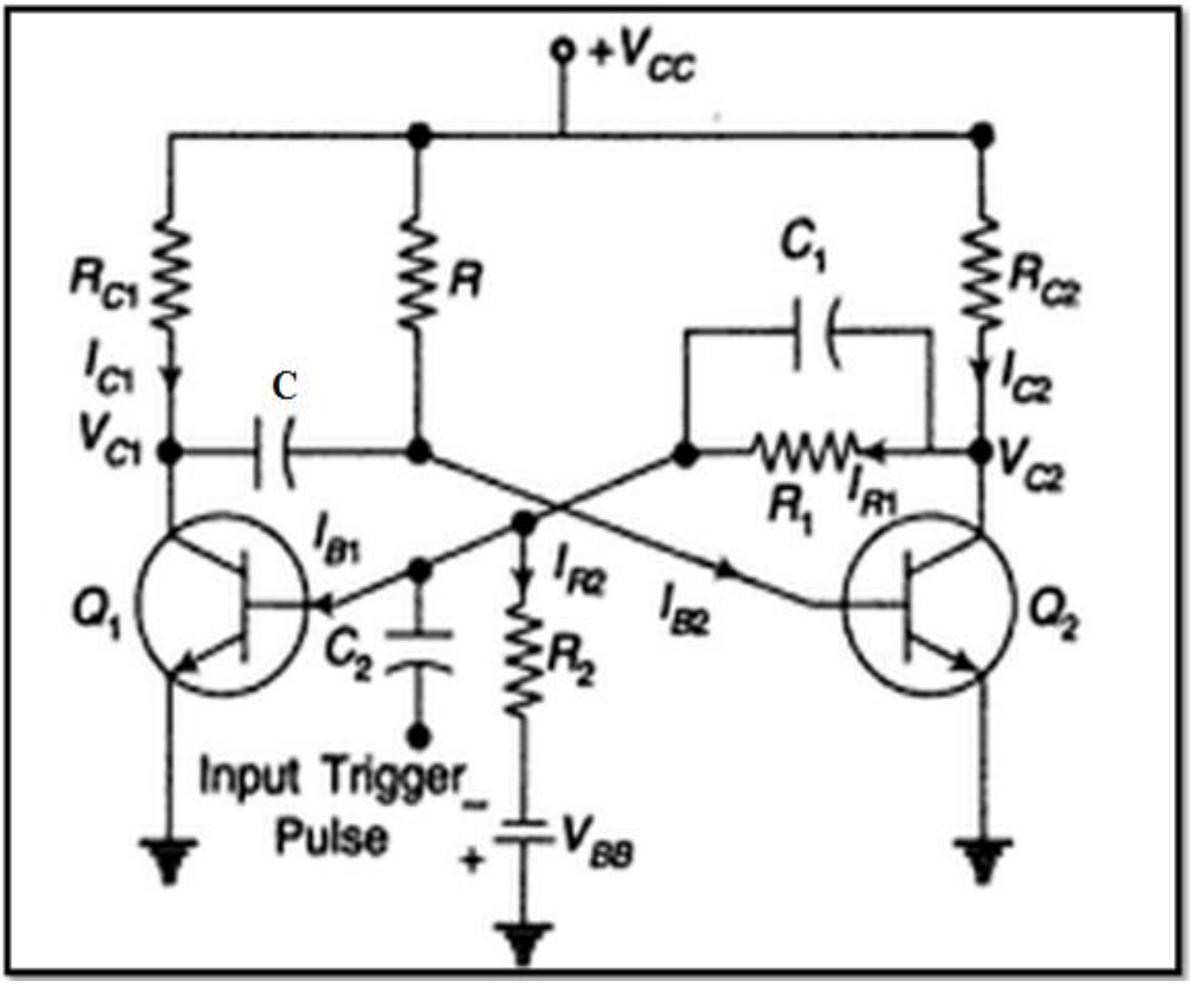
Thus the collector coupled astable multivibrator was designed and tested.

Multivibrator circuit	Theoretical frequency	Practical frequency

MARKS ALLOCATION		
Experimental Setup	10	
Execution	10	
Viva	10	
Total	30	

CIRCUIT DIAGRAM

MONO STABLE MULTIVIBRATR



Ex. No:
Date:

MONO STABLE MULTIVIBRATOR

AIM

To design and construct Mono stable multivibrator using transistor

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Transistor	BC 547	2
3.	Resistor		
4.	Capacitor		
5.	Bread board	-	1
6.	Power supply	(0-30)V	1

THEORY

The monostable multivibrator (sometimes called a ONE-SHOT MULTIVIBRATOR) is a square- or rectangular-wave generator with just one stable condition. With no input signal (quiescent condition) one amplifier conducts and the other is in cutoff. The monostable multivibrator is basically used for pulse stretching. It is used in computer logic systems and communication navigation equipment.

The operation of the mono stable multivibrator is relatively simple. The input is triggered with a pulse of voltage. The output changes from one voltage level to a different voltage level. The output remains at this new voltage level for a definite period of time. Then the circuit automatically reverts to its original condition and remains that way until another trigger pulse is applied to the input. The mono stable multivibrator actually takes this series of input triggers and converts them to uniform square pulses.. All of the square output pulses are of the same amplitude and time duration.

DESIGN

Given output pulse 700 ns

$h_{fe(min)}$ = 100 ; $I_{C\,(sat)}$ = 1 mA; V_{CC} = ±12V ; $V_{CE(Sat)}$ = 0.3V

R_{C2}=R_{C1}= (V_{CC}- $V_{CE(sat)}$) / I_{C1}($_s$at)

Find R_{C1} =

$I_{B2(sat)}$ = $I_{C2(sat)}$ / $h_{fe(min)}$

R_B = V_{CC} – $V_{BE(sat)}$ / $_{IB2(sat)}$

At quasi stable state Q1- on , Q2-off

I_2 = I_C/10

V_{R2} = $V_{BE(sat)}$

R_2=V_{R2}/I_2

From the circuit

R_{C2} + R_1 = (V_{CC} – $V_{BE(sat)}$) / (I_{B1}+I_2)

Find R1 =

Time period expression: (T= 700ns)

Time period: T = 0693 R_B * C

Find C = ?

For Speed up capacitor C_1 choosen such that R_1 C_1 =1ms

Therefore: **C_1 = 1ms / R_1**

CONSTRUCTION

- It contains one stable state and one quasi stable state.
- It needs the external pulse to change their permanent state to quasi-stable state and return back to permanent state after completing RC time constant.
- Also called One short, single short, one swing multivibrator.
- Two transistors Q_1 and Q_2 used and both are connected back to back.
- R_BC_1 acts as a timing circuit.
- Trigger pulse applied to base of transistor $Q_1$to change the state.

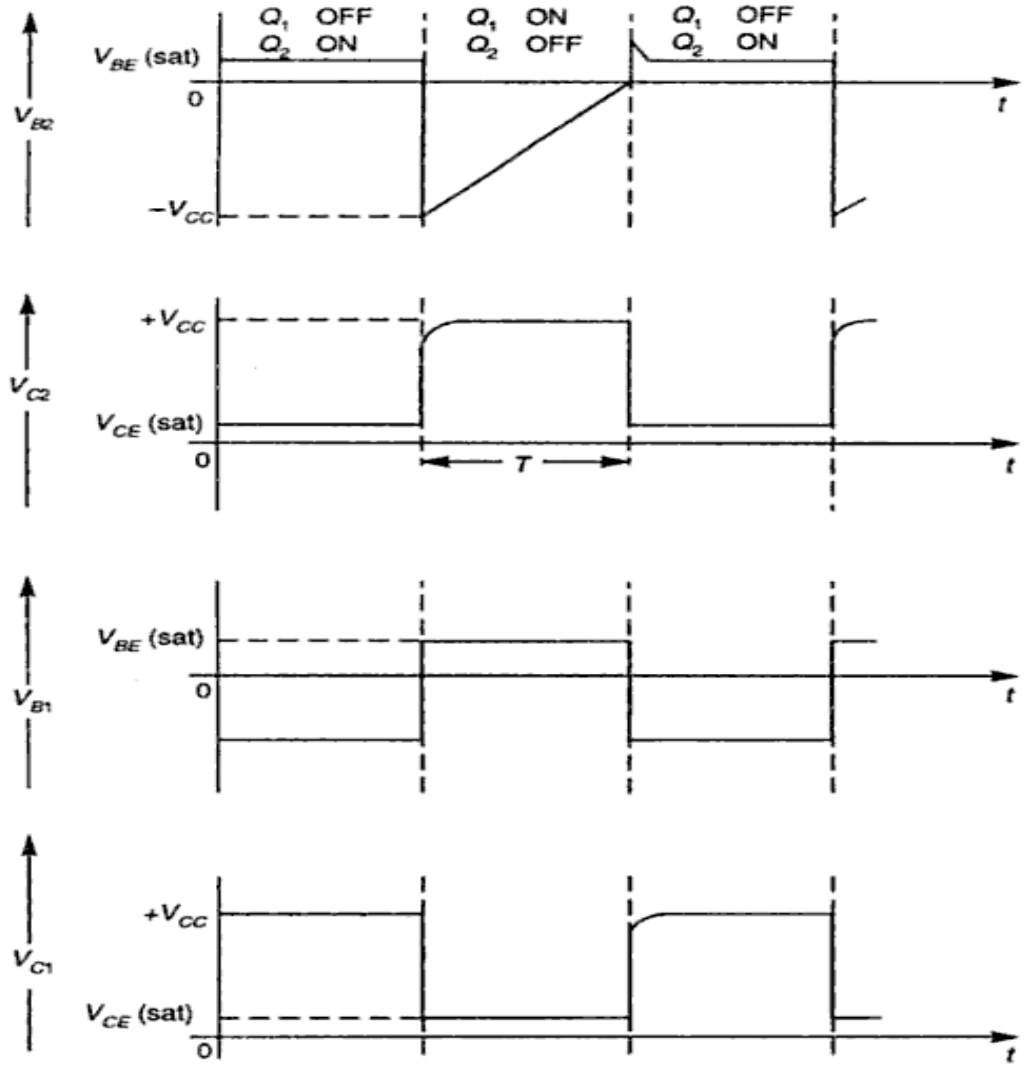
PROCEDURE

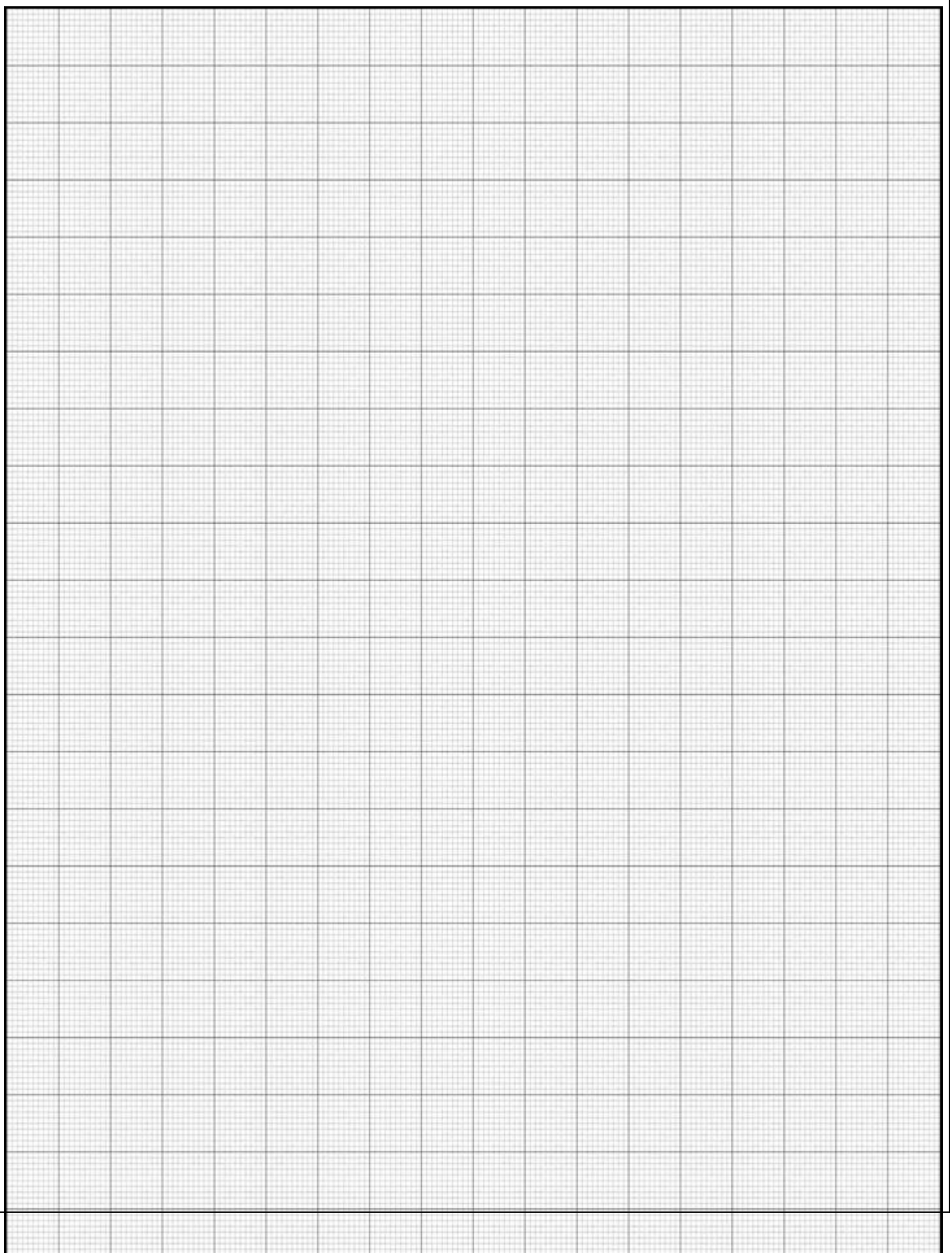
1. The circuit diagram is given as per circuit diagram
2. The dc supply is switched ON
3. The collector terminal of transistor connected to CRO
4. The output voltage and time period are measured across transistors Q1 & Q2 at both the emitter and collector
5. The waveforms are plotted on a graph

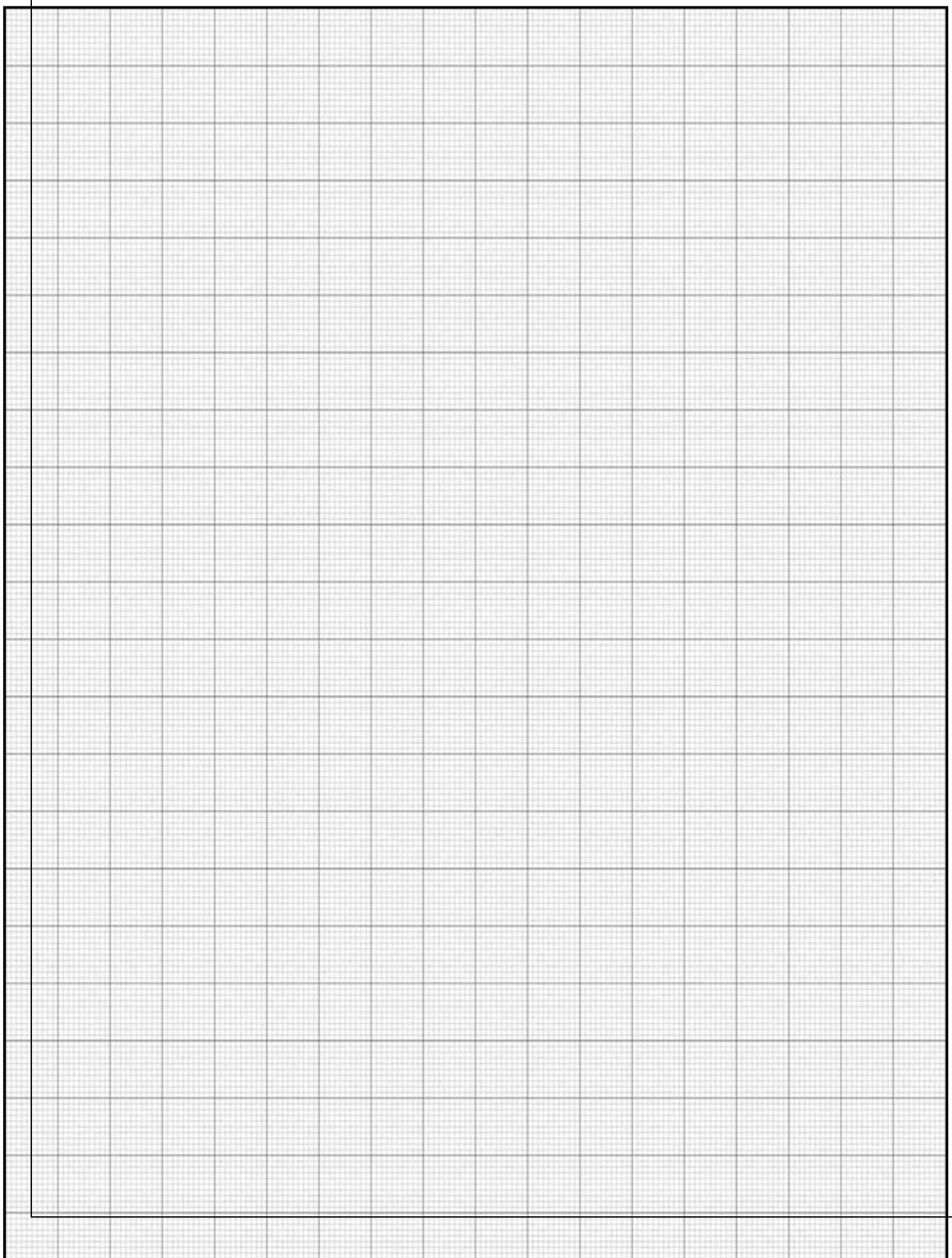
OBSERVATION

S.No	Parameters	Across Q1	Across Q2
1	V_{CC}		
2	$V_{CE(SAT)}$		
3	Time on		
4	Time off		
5	Total time		
6	Frequency		

MODEL GRAPH







REVIEW QUESTIONS:

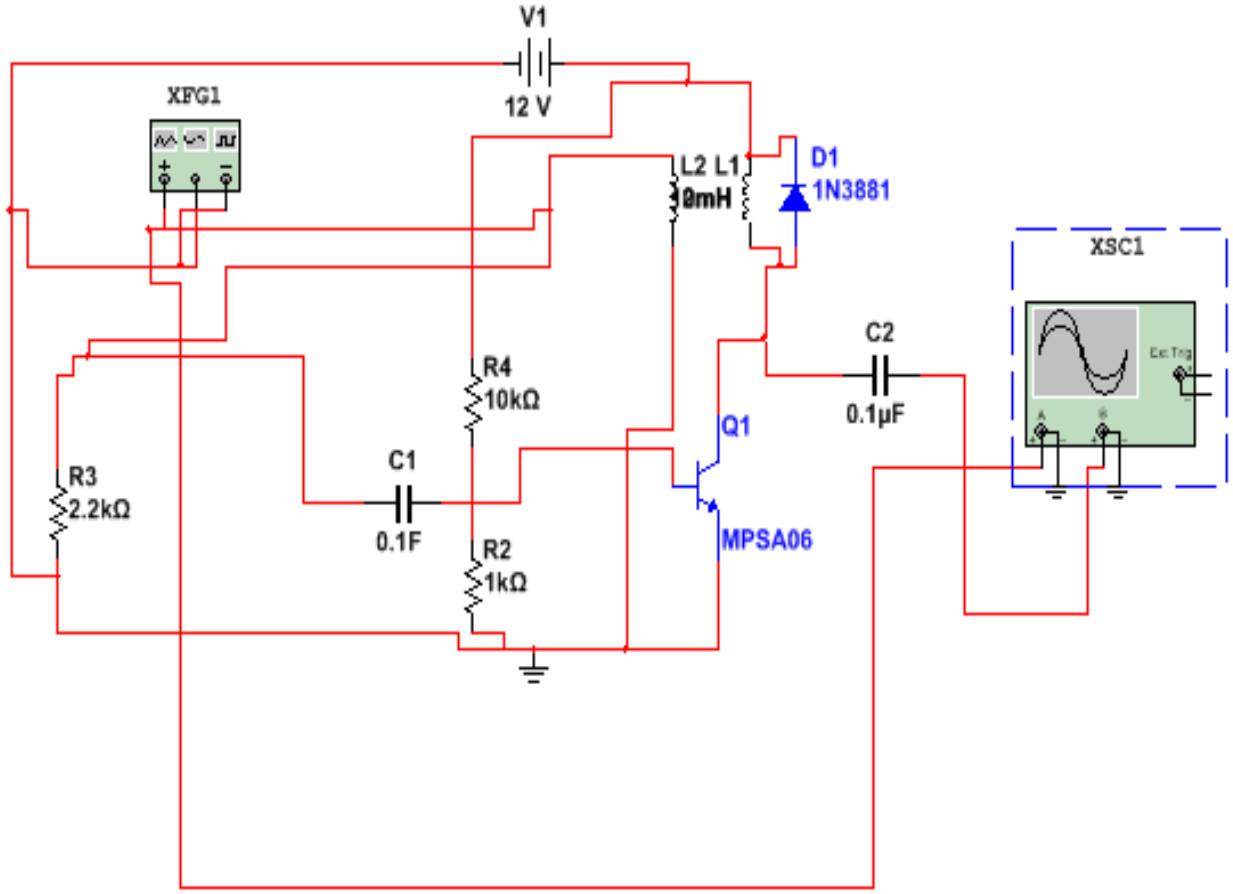
1. What is the origin of the name monostable multivibrator?
2. Why is monostable multivibrator often called one-shot circuit?
3. What is the application of monostable multivibraotr?

RESULT:

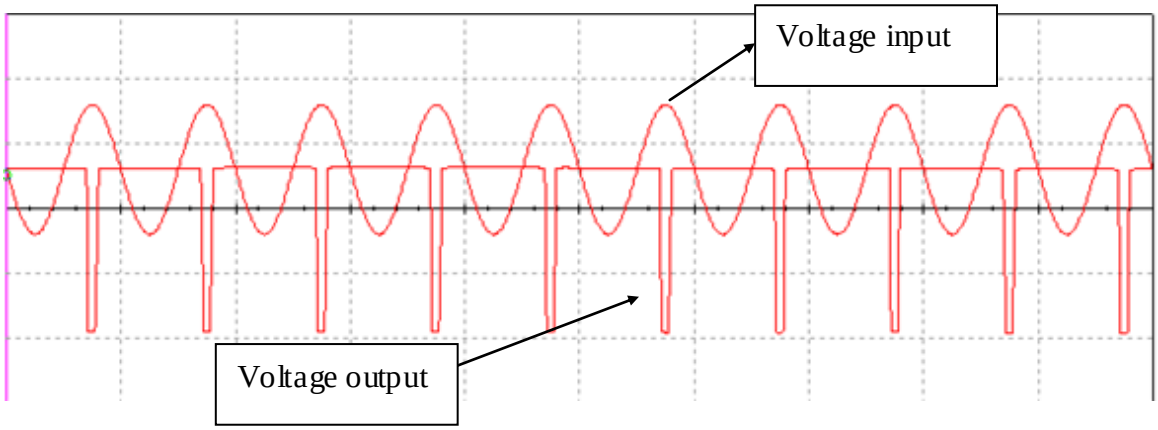
Thus the monostable multivibrator is designed and the output waveform is plotted.

MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	

CIRCUIT DIAGRAM FOR FREE RUNNING BLOCKING OSCILLATORS



MODEL GRAPH:



Ex. No:
Date:

FREE RUNNING BLOCKING OSCILLATORS

AIM

To design and construct free running blocking oscillator circuit and observe its waveforms.

APPARATUS & COMPONENTS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1.	CRO	(0-30) MHz	1
2.	Transistor	MPSA06	1
	Diode	1N3881	1
3.	Resistor		
4.	Function generator		
5.	Capacitor		
6.	Bread board	-	1
7.	Power supply	(0-30)V	1

THEORY

The BLOCKING OSCILLATOR is a special type of wave generator used to produce a narrow pulse, or trigger. Blocking oscillators have many uses, most of which are concerned with the timing of some other circuit. They can be used as frequency dividers or counter circuits and for switching other circuits on and off at specific times.

In a blocking oscillator the pulse width (pw), pulse repetition time (prt), and pulse repetition rate (prr) are all controlled by the size of certain capacitors and resistors and by the operating characteristics of the transformer. The circuit is called a free-running blocking oscillator. When it is desired to synchronize or otherwise control the pulse repetition rate, an external "trigger" pulse is applied to the blocking oscillator grid or cathode.

Blocking oscillators are used to obtain pulses at certain repetition rates. The pulse may be used to drive a pulse amplifier, or it may be used to modulate a *UHF* oscillator.

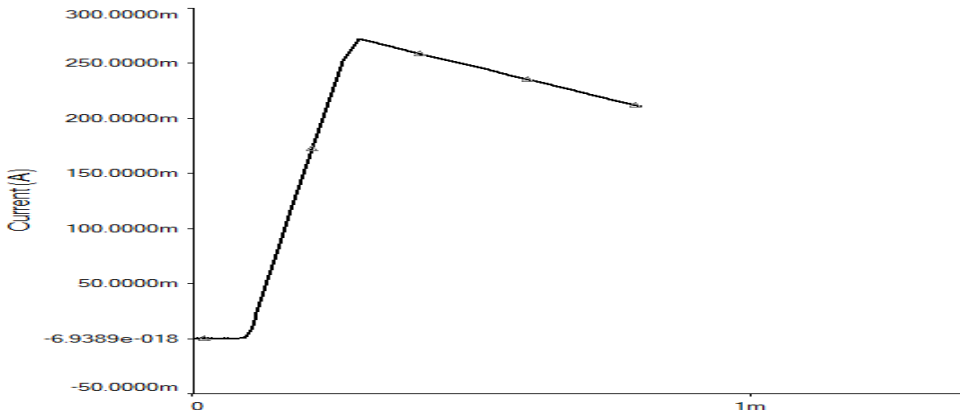
TABULATION:

PARAMETER	Output voltage
Amplitude	
Time Period	

Transient Analysis:

Magnetizing current(Im) in mA	Time Period in secs

TRANSIENT ANALYSIS MODEL GRAPH



PROCEDURE

1. The connection is given as per circuit diagram
2. The dc supply is switched ON
3. The collector terminal of transistor connected to CRO
4. The output voltage and time period are measured across transistor Q1 at the collector.
5. The waveforms are plotted on a graph.

REVIEW QUESTIONS:

1.What is a blocking oscillator?

2.What are the types of blocking oscillator?

3.How many stable states are there in free running blocking oscillator?

RESULT:

Thus the free running blocking oscillator is designed and the output waveform is plotted.

MARKS ALLOCATION		
Experimental Setup	**10**	
Execution	**10**	
Viva	**10**	
Total	**30**	