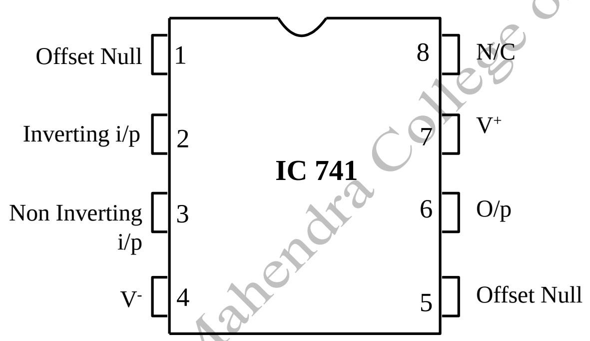
# STUDY OF OP-AMP

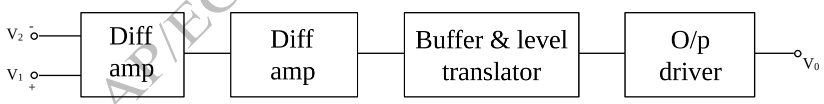
An operational amplifier or op-amp is a linear integrated circuit that has a very high voltage gain, high input impedance and low output impedance. Op-amp is basically a differential amplifier whose basic function is to amplify the difference between two input signals.

Op-amp has five basic terminals, that is, two input terminals, one o/p terminal and two power supply terminals. Pin2 is called the inverting input terminal and it gives opposite polarity at the output if a signal is applied to it. It produces a phase shift of $180^o$ between input and output. Pin3 is called the non-inverting terminal that amplifies the input signal without inversion, i.e., there is no phase shift or i/p is in phase with o/p. The op-amp usually amplifies the difference between the voltages applied to its two input terminals. Two further terminals pins 7 and 4 are provided for the connection of positive and negative power supply voltages respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates ‘No Connection’.

**Study of op-amp**




**Block schematic of op-amp**




The block diagram of op-amp shows two difference amplifiers, a buffer for less loading, a level translator for adjusting operating point to original level and o/p stage. An ideal op-amp should have the following characteristics:

1. Infinite bandwidth
2. Infinite input resistance
3. Infinite open loop gain
4. Zero output resistance
5. Zero offset.

Op-amps have two operating configurations; open loop and closed loop. In open loop configuration, it can operate as a switch but gain is uncontrolled. In closed loop configuration, gain can controlled by feed back resistance $R_f$ and input resistance $R_{in}$.

**EX.No:**

# DESIGN AND TESTING OF INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS

**Aim:**

To design Inverting, Non-inverting and differential amplifiers using op-amp and test its performance.

**Apparatus required:**

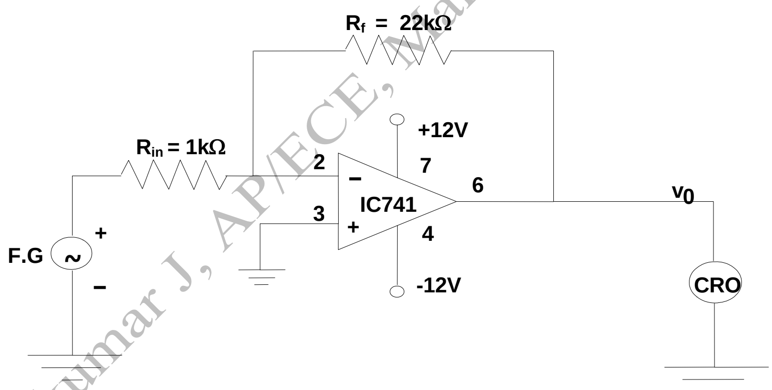
| S.No | Components | Range | Quantity |
|---|---|---|---|
| 1. | Op-amp | IC 741 | 1 |
| 2. | Dual trace supply | (0-30) V | 1 |
| 3. | Function Generator | (0-1) MHz | 1 |
| 4. | Resistors | | |
| 5. | Capacitors | | |
| 6 | CRO | (0-30) MHz | 1 |

**a) Inverting amplifier: [Closed Loop Configuration]**

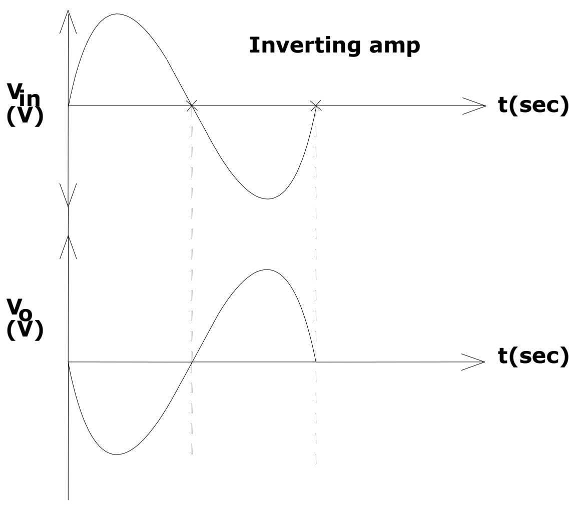
**Design:**

$A_{CL} = V_o/V_{in} = - R_f / R_{in}$;
Assume $A_{CL} = 20$
=> $- R_f / R_{in} = -20$
Now Assume $R_f = 22k\Omega$; => $R_{in} = 1.1k\Omega \approx 1k\Omega$

**Circuit Diagram:**




**Model Graph:**



**b) Non inverting amplifier: [Closed Loop Configuration]**

**Design:**

$A_{CL} = V_o / V_{in} = 1 + R_f / R_{in}$;

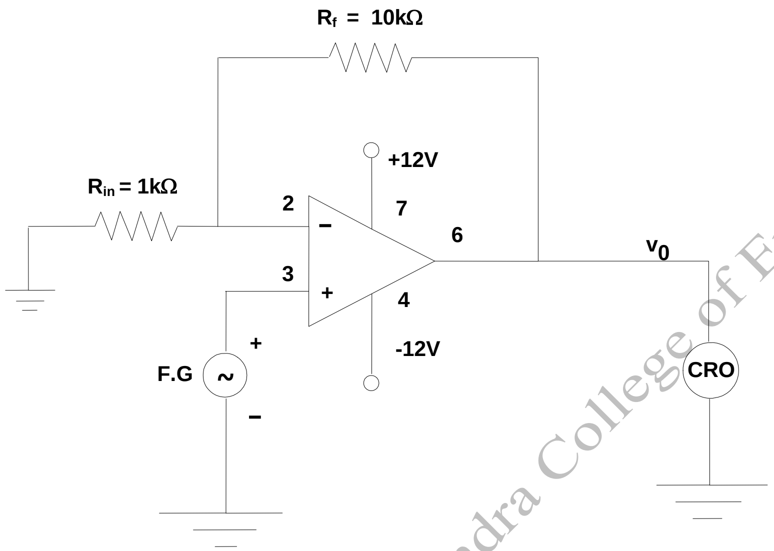
Assume $A_{CL} = 10$;

=> $10 = 1 + R_f / R_{in}$

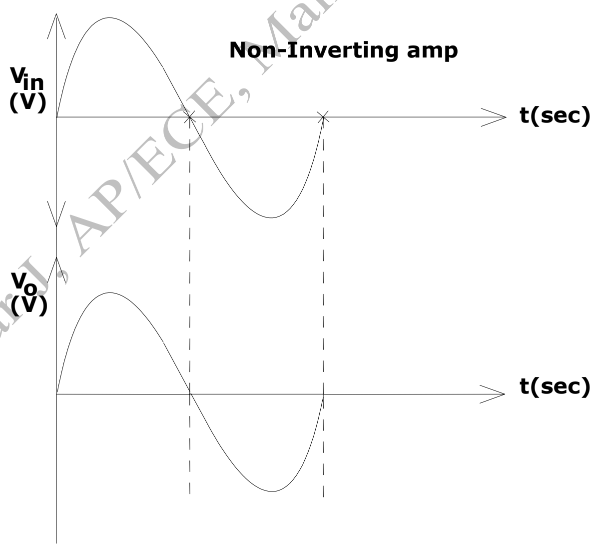
Assume $R_f = 10k\Omega$;

=> $R_{in} = 1.1k\Omega \approx 1k\Omega$

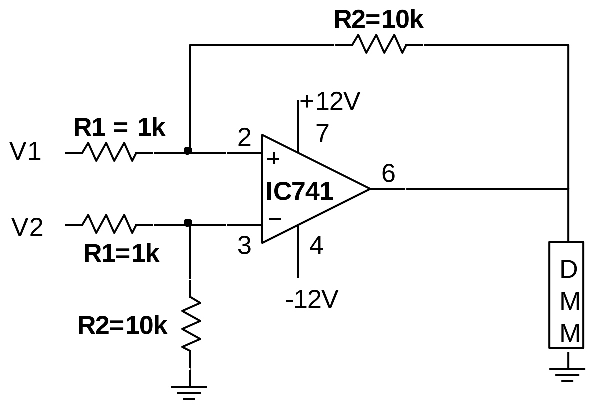
**Circuit Diagram**




**Model Graph:**



**b) Differential Amplifier: [Closed Loop Configuration]**




**Result:**

Thus Inverting, Non-inverting and Differential amplifier using op-amp was designed and tested.

**EX.No:**

## DESIGN AND TESTING OF INTEGRATOR AND DIFFERENTIATOR

**Aim:**

To design Integrator and Differentiator using op-amp and test its performance.

**Apparatus required:**

| S.No | Components | Range | Quantity |
|---|---|---|---|
| 1. | Op-amp | IC 741 | 1 |
| 2. | Dual trace supply | (0-30) V | 1 |
| 3. | Function Generator | (0-1) MHz | 1 |
| 4. | Resistors | | |
| 5. | Capacitors | | |
| 6 | CRO | (0-30) MHz | 1 |

**a) Differentiator:**

**Design:**

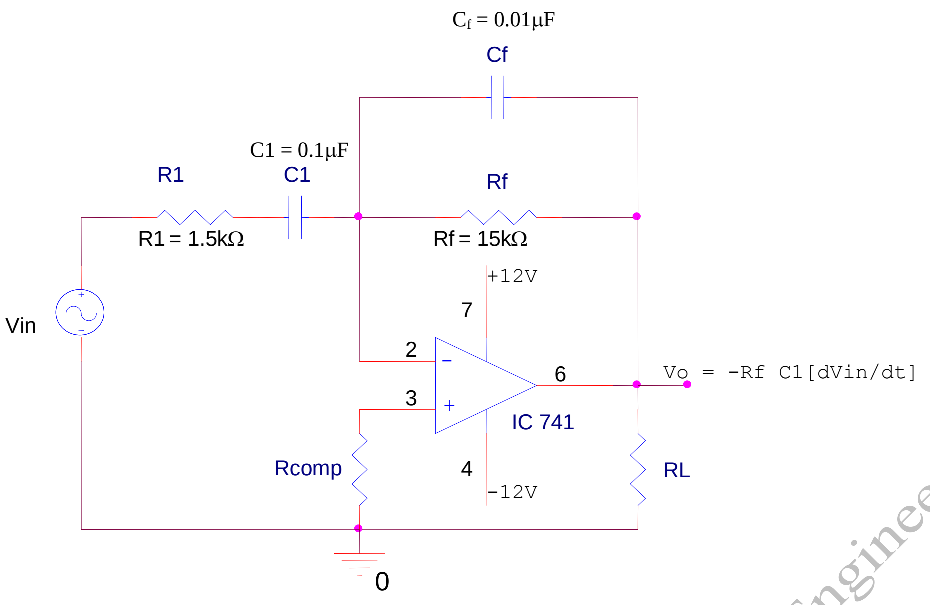
Step1: Select $f_a$ equal to the highest frequency of the input signal to be differentiated. Then assuming a value of $C_1 < 1\mu F$. Calculate the value of $R_f$.

Step2: Choose $f_b = 20 f_a$ and calculate the values of $R_1$ and $C_f$ so that $R_1C_1 = R_f C_f$.

$f_a$ = ______KHz ; $f_b$ = ______KHz ;$C_1 = 0.1\ \mu f$; $R_{COMP} = R_f$ ; $R_L = 10K\Omega$

$f_a = 1/ [2\pi R_f C_1]$; $R_f = 1/2\pi\ C_1\ f_a$ ; $f_b = 1/ [2\pi R_1C_1]$;$R_1 = 1/2\pi\ C_1\ f_b$;$R_1C_1 = R_f C_f$; $C_f = R1C1/ R_f$

## Circuit Diagram




## Observation:

For sine wave input:

Peak to peak amplitude of the input = volts.

Frequency of the input = Hz

Peak to peak amplitude of the output = volts.

Frequency of the output = Hz

For square wave input:

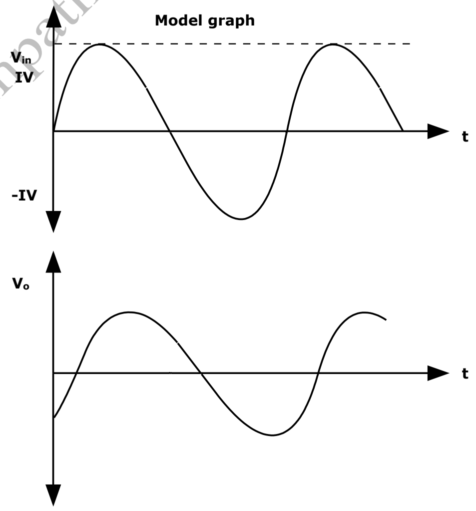
Peak to peak amplitude of the input = volts.

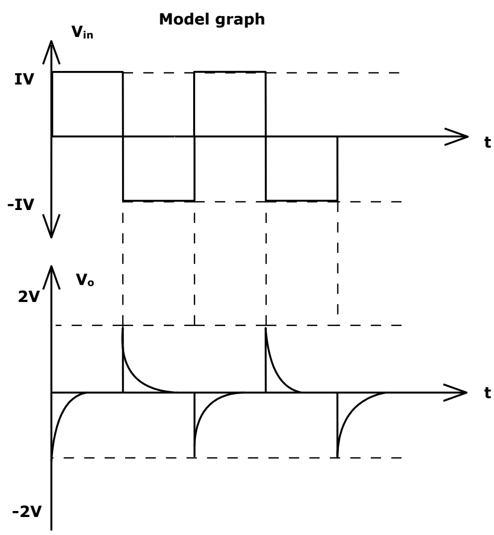
Frequency of the input = Hz

Peak to peak amplitude of the output = volts.

Frequency of the output = Hz

## Model Graph:



## b) Integrator:

### Design:

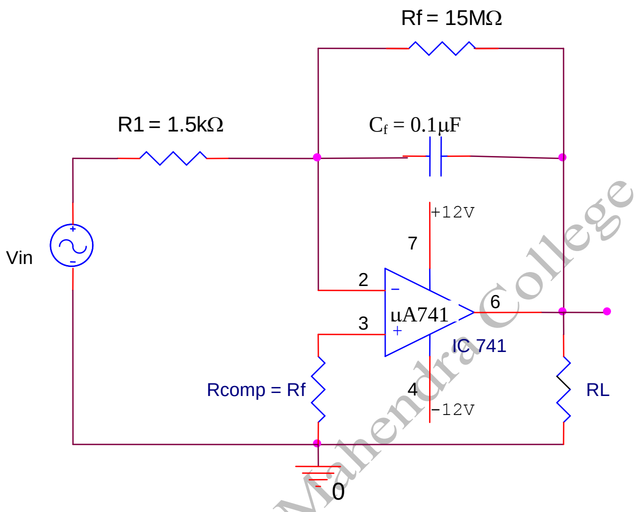
Generally the value of the $f_a$ and in turn $R_1C_f$ and $R_f\,C_f$ values should be selected such that $f_a < f_b$. From the frequency response we can observe that $f_a$ is the frequency at which the gain is 0 db and $f_b$ is the frequency at which the gain is limited. Maximum input signal frequency = 1 KHz.

Condition is time period of the input signal is larger than or equal to $R_f\,C_f$ (i.e.) $T \geq R_1C_f$

$f_b$ = ______KHz ; $f_a = f_b/10$; $R_f = 10R_1$; $R_{COMP} = R_1$; $R_L$ & $R_1 = 10K\Omega$

$f_a = 1/\,[2\pi R_fC_f]$; $Rf\,C_f$ = 1msec &; Cf = 1msec/100K

### Circuit Diagram:




$V_O = -\,[1/R_1C_f]\int Vin\,dt$

### Observation:

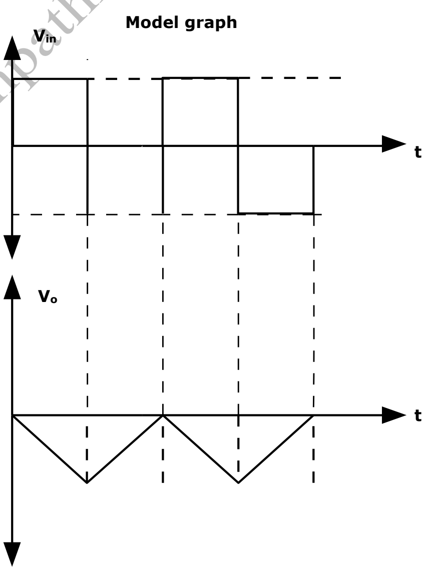
For sine wave input:

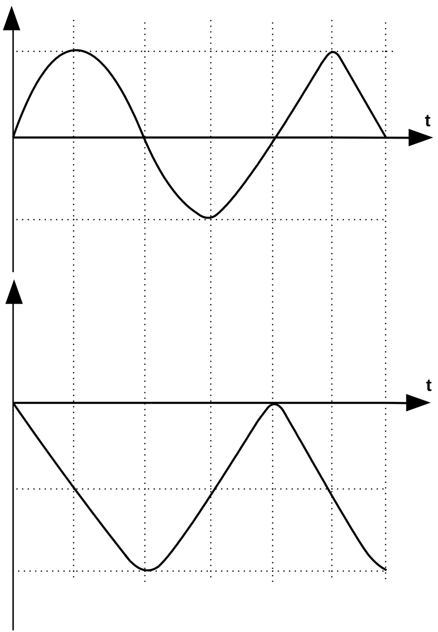
Peak to peak amplitude of the input = volts.
Frequency of the input = Hz
Peak to peak amplitude of the output = volts.
Frequency of the output = Hz

For square wave input:

Peak to peak amplitude of the input = volts.
Frequency of the input = Hz
Peak to peak amplitude of the output = volts.
Frequency of the output = Hz

### Model Graph:



**Result:**

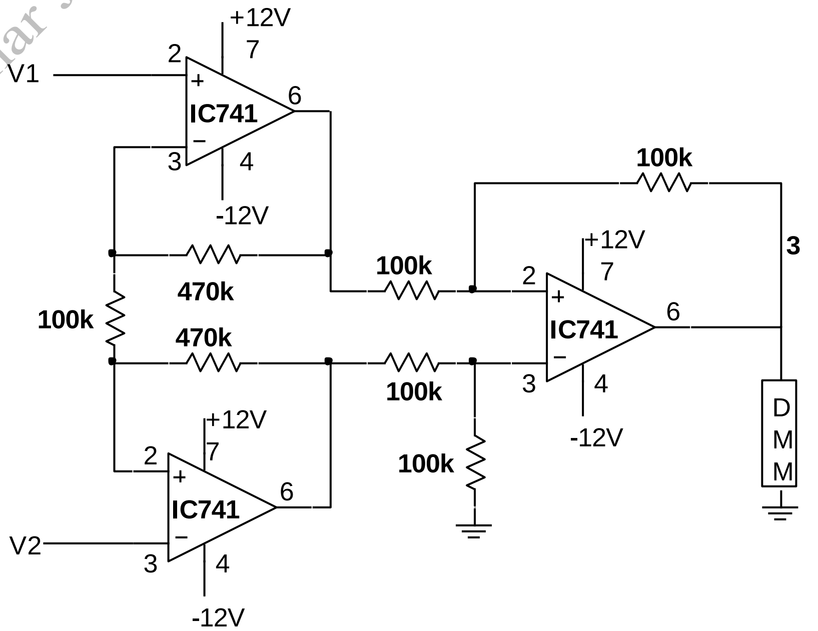
Thus Integrator and Differentiator using op-amp was designed and tested.

**EX.No:**

## DESIGN AND TESTING OF INSTRUMENTATION AMPLIFIER

**AIM:**

To design and test the operation of Instrumentation Amplifier for various gain values.



**APPARATUS REQUIRED :**
i. IC 741 – 3 NO.
ii. Resistors
iii. RPS, DMM

**THEORY :**

Instrumentation amplifier is an amplifier that realizes high input impedance and very low offset and drift voltage values. This configuration is better than inverting or non-inverting amplifier because it has minimum non-linearity, stable voltage gain and high CMRR ( > 100 dB.). This type of amplifier is used in thermocouples, strain gauges and biomedical probes.

Output voltage

$$V_o = \frac{R_2}{R_1}\left[1 + \frac{2R'}{R}\right](V_2 - V_1)$$

$$\text{Gain} = \frac{R_2}{R_1}\left[1 + \frac{2R'}{R}\right]$$



**PROCEDURE:**
(i) Connect the instrumentation amplifier circuit.
(ii) For various input voltage $V_1$ and $V_2$ measure and record the output voltage and tabulate.

**TABULAR COLUMN:** $R = R' = 1K\Omega$

| S.No. | R2 ohms | R1 ohms | V1 volts | V2 volts | $V_o = \frac{R_2}{R_1}\left[1 + \frac{2R'}{R}\right](V_2 - V_1)$ | |
|---|---|---|---|---|---|---|
| | | | | | theoretical | practical |
| 1. | 2.2K | 1K | 2 | 1 | | |
| 2. | 2.2K | 1K | 3 | 2 | | |
| 3. | 1K | 1K | 4 | 2 | | |
| 4. | 1K | 1K | 2 | 5 | | |
| 5. | 2K | 1K | 1 | 4 | | |

**RESULT:**

Thus the instrumentation amplifier is designed, constructed and tested

**Ex. No**

## Astable and Monostable Multivibrators using op-amp

## Aim

To design Astable and monostable Multivibrators & Schimitt Trigger using op-amp and to plot its waveforms.

## Apparatus Required:

| S.No | Component | Range | Quantity |
|---|---|---|---|
| 1. | Op amp | IC 741 | 1 |
| 2. | DTS | (0-30) V | 1 |
| 3. | CRO | | 1 |
| 4. | Resistor | | 1 |
| 5. | Capacitors | – | – |
| 6. | Diode | IN4001 | 2 |
| 7. | Probes | – | 1 |

## Design:

### 1. Monostable Multivibrators:

$\beta = R_2/R_1+R_2$ [$\beta = 0.5$ & $R_1 = 10$ K]

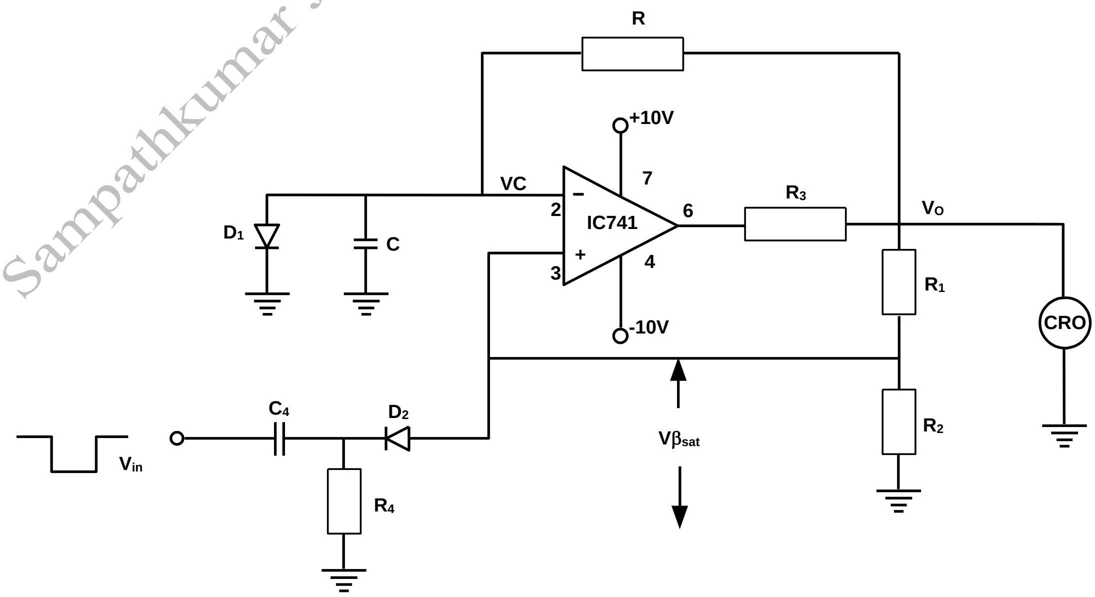
Find $R_2$ = ; R3 = 1K; R4 = 10K;

Let F =_____KHz ; C= 1mfd; C4 = 0.1mfd

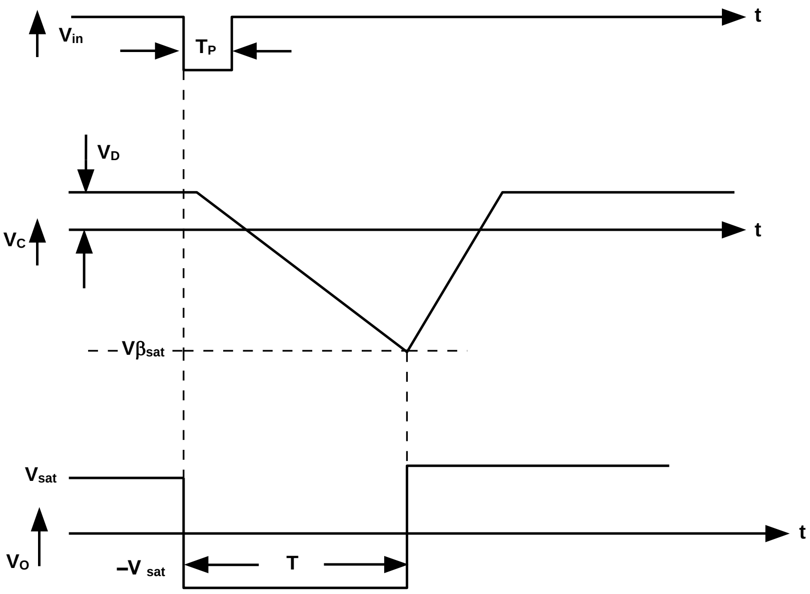
Pulse width, T = 0.69RC

Find R =

## Circuit Diagram



**Model graph:**




**Procedure:**

1. Make the connections as shown in circuit diagram.
2. A trigger pulse is given through differentiator circuit through pin no.3
3. Observe the pulse waveform at pin no.6 using CRO and note down the time period.
4. Plot the waveform on the graph.

**2. Astable Multivibrators:**

**Design:**

$$T = 2RC$$

$$R_1 = 1.16\ R_2$$

Given $f_O$ = _______KHz

Frequency of Oscillation fo = 1 / 2 RC if $R_1 = 1.16R_2$

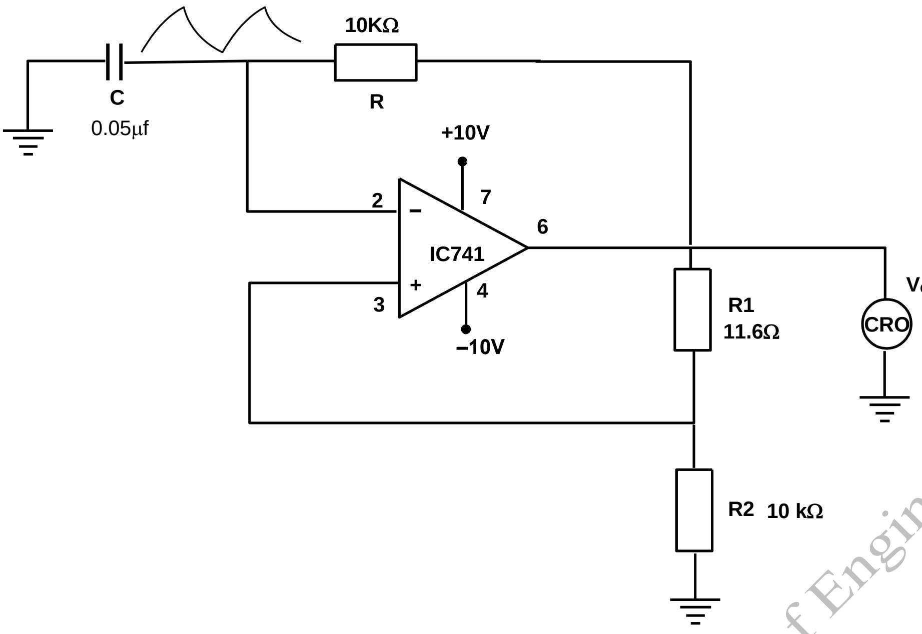
Let $R_2$ = 10 KΩ

$R_1 = 10 * 1.16 = 11.6$KΩ

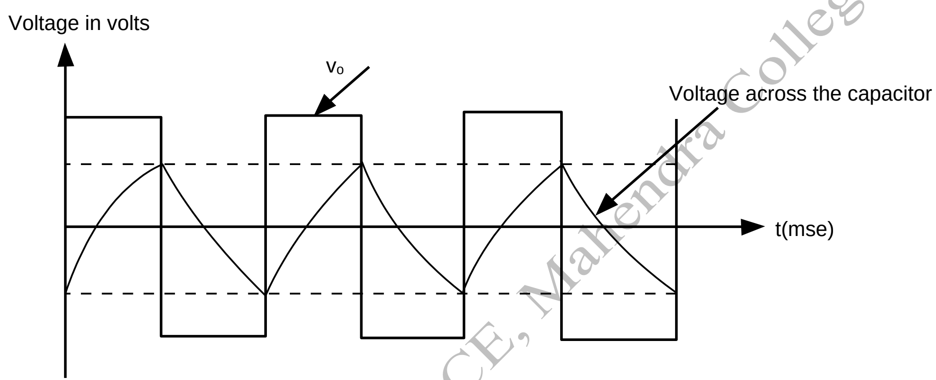
Let C = 0.05 µF

$R = 1 / 2\ fC = 1/ (2 * 1 * 10^3 * 0.05 * 10^{-6}) =$

## Circuit Diagram




## Model graph




## Procedure:

1. Make the connections as shown in the circuit diagram
2. Keep the CRO channel switch in ground and adjust the horizontal line on the x axis so that it coincides with the central line.
3. Select the suitable voltage sensitivity and time base on the CRO.
4. Check for the correct polarity of the supply voltage to op-amp and switch on power supply to the circuit.
5. Observe the waveform at the output and across the capacitor. Measure the frequency of oscillation and the amplitude. Compare with the designed value.
6. Plot the Waveform on the graph.

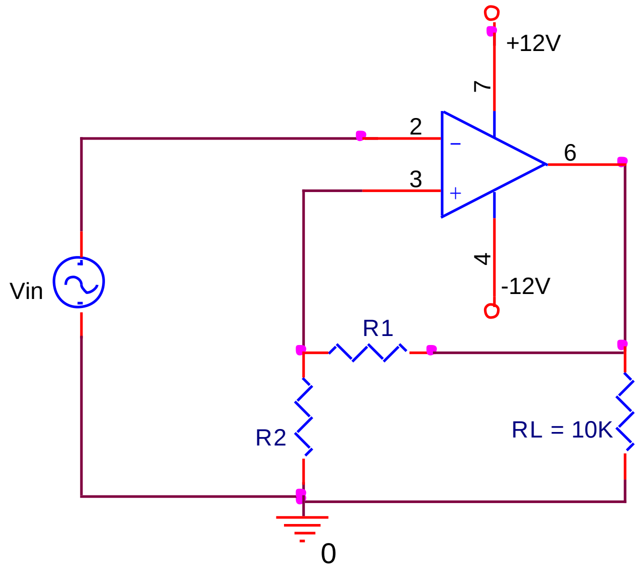
## 3) Schmitt Trigger:

### Design

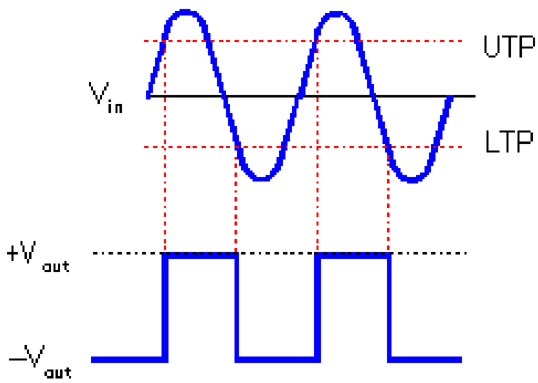
$V_{CC}$ = 12 V; $V_{SAT}$ = 0.9 $V_{CC}$**;** R1= 47KΩ; R2 = 120Ω

$V_{UT}$ = + [$V_{SAT}$ $R_2$] / [$R_1$+$R_2$] & $V_{LT}$ = - [$V_{SAT}$ $R_2$] / [$R_1$+$R_2$] & HYSTERSIS [H] = $V_{UT}$ **-** $V_{LT}$

## Circuit Diagram




## Model Graph




## Procedure

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than $V_{cc}$)
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode and switch the trigger source in CRO to CHI.
5. Plot the input and output waveforms on the graph.

## Observation:

Peak to peak amplitude of the output = Volts.

Frequency = Hz.

Upper threshold voltage = Volts.

Lower threshold voltage = Volts.

## Result:

Thus Astable & Monostable Multivibrators and Schimitt trigger were designed using op-amp and the waveforms were plotted

**EXP.NO:**

## MULTIVIBRATORS USING IC 555

**Aim:**

To design and test an Astable and Monostable Multivibrators using 555 timer with duty cycles ratio.

**Apparatus Required:**

| S.No | Component | Range | Quantity |
|---|---|---|---|
| 1. | 555 TIMER | | 1 |
| 2. | Resistors | 3.3K, 6.8k | 1 |
| 3. | Capacitors | 0.1 μ F, 0.01μ F | 2 |
| 4. | Diode | In4001 | 1 |
| 5. | CRO | | 1 |
| 6. | Power supply | ± 15 V | 1 |
| 7. | Probe | | 2 |
| 8. | Bread Board | | 1 |



**Astable Multivibrators using 555**

Fig shows the 555 timer connected as an Astable Multivibrators. Initially, when the output is high. Capacitor C starts charging towards $V_{cc}$ through $R_A$ and $R_B$. As soon as capacitor voltage equals 2/3 $V_{cc}$ upper comparator (UC) triggers the flip flop and the output switches low. Now capacitor C starts discharging through $R_B$ and transistor $Q_1$.

When the voltage across C equals 1/3 $V_{cc}$ lower comparator (LC), output triggers the flip-flop and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between 2/3 $V_{cc}$ and 1/3 $V_{cc}$ respectively. The time during which the capacitor charges form 1/3 $V_{cc}$ to 2/3 $V_{cc}$ is equal to the time the output is high and is given by

$$T_c = 0.69(R_A+R_B)C \qquad (1)$$

Where $R_A$ and $R_B$ are in Ohms and C is in farads. Similarly the time during which the capacitor discharges from 2/3 $V_{cc}$ to 1/3 $V_{cc}$ is equal to the time the output is low and is given by

$$T_d = 0.69\ R_B\ C \qquad (2)$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69\ (R_A + 2R_B)\ C} \qquad (3)$$

The frequency of oscillation

$$f_o = 1 / T = 1.45 / (R_A+2R_B)C \qquad (4)$$

Eqn (4) shows that fo is independent of supply voltage Vcc

The duty cycle is the ratio of the time $t_d$ during which the output is low to the total time period T. This definition is applicable to 555 Astable Multivibrators only; conventionally the duty cycle ratio is defined as the ratio as the time during which the output is high to the total time period.

$$\therefore \text{ Duty cycle} = t_d \; T \times 100$$

$$R_B + R_A + 2R_B \times 100 \qquad (5)$$

To obtain 50% duty cycle a diode should be connected across $R_B$ and $R_A$ must be a combination of a fixed resistor and a potentiometer. So that the potentiometer can be adjusted for the exact square waves

**DESIGN:**

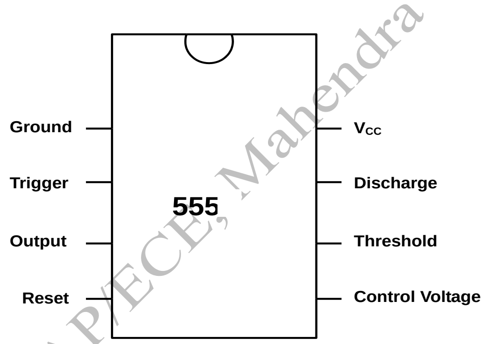
Design an Astable Multivibrators for a frequency of ______KHz with a duty cycle ratio of D = 50 %**fo = 1/T = 1.45 / ($R_A$+2$R_B$)C**

Choosing C = 1 μF; $R_A$ = 560

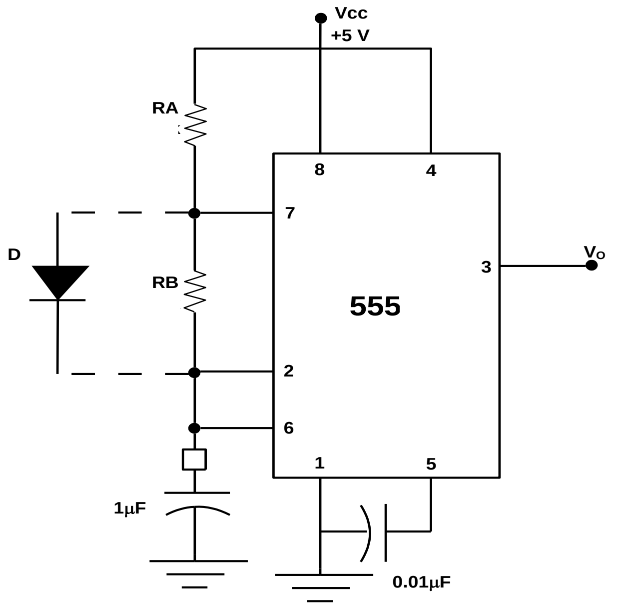
$D = R_B / R_A + 2R_B = 0.5$ [50%]

$R_B$ = ______

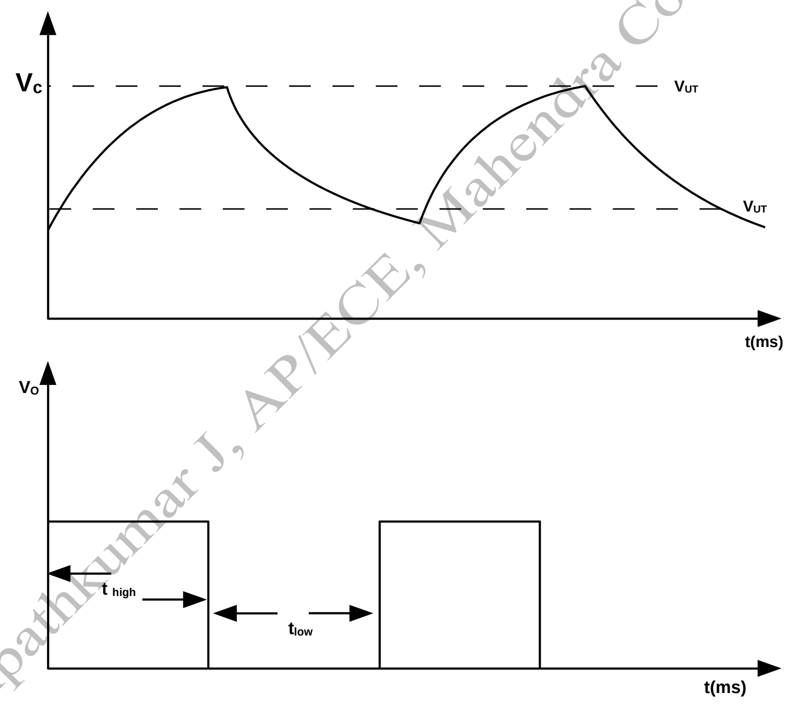
**Pin diagram:**



## Circuit Diagram




## Model Graph






## Procedure:

1. Rig-up the circuit of 555 Astable Multivibrators as shown in fig with the designed value of components.
2. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
3. Switch on the power supply to CRO and the circuit.

4. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings and frequency.
5. Switch off the power supply. Connect a diode across $R_B$ as shown in dashed lines in fig to make the Astable with 50 % duty cycle ratio. Switch on the power supply. Observe the output waveform. Draw to scale on a graph sheet.

**Monostable Multivibrators using 555**

Monostable Multivibrators has one stable state and other is a quasi stable state. The circuit is useful for generating single output pulse at adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components, resistor and a capacitor.

The stable state is the output low and quasi stable state is the output high. In the stable state transistor Q1 is ‘on’ and capacitor C is shorted out to ground. However upon application of a negative trigger pulse to pin2, Q1 is turned ‘off’ which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards $V_{cc}$ through $R_A$. However when the voltage across C equal 2/3 $V_{cc}$ the upper comparator output switches form low to high which in turn drives the output to its low state via the output of the flip flop. At the same time the output of the flip flop turns Q1 ‘on’ and hence C rapidly discharges through the transistor. The output remains low until a trigger is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 Vcc. The width of the output pulse is given by,

$$T = 1.1\, R_A C$$

**Design:**

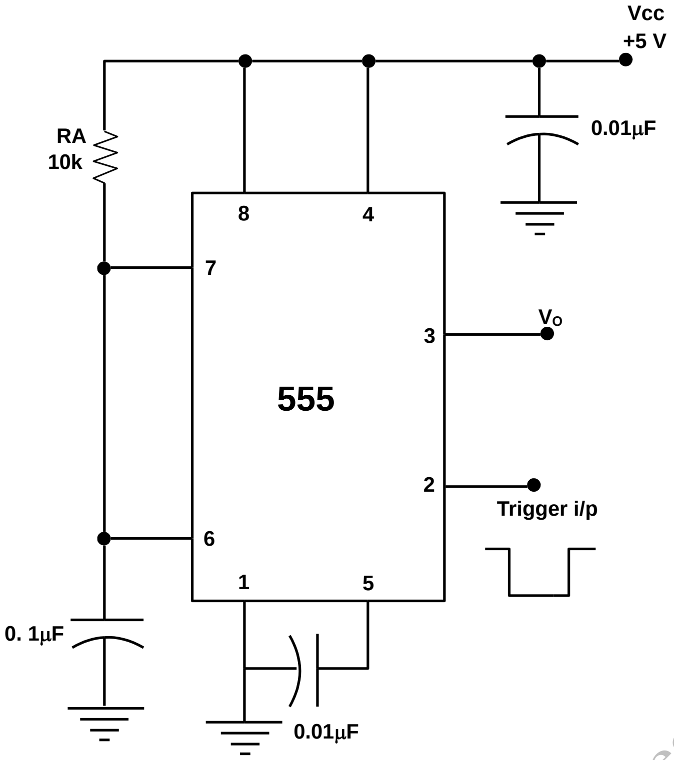
Given a pulse width of duration of 100 μs

Let C = 0.01 mfd; F = _________KHz

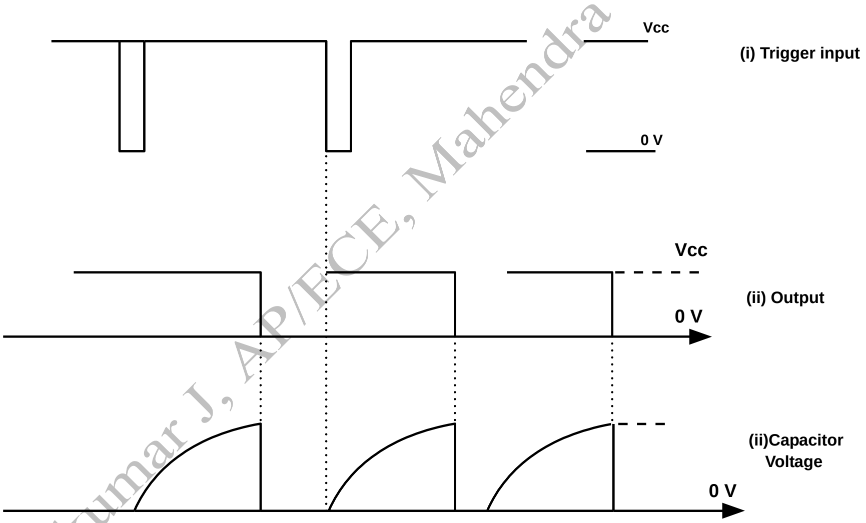
Here, T= 1.1 $R_A$C

So, $R_A$ =

**Circuit Diagram:**




**Model Diagram:**




**Procedure:**

1. Rig-up the circuit of 555 monostable Multivibrators as shown in fig with the designed value of components.
2. Connect the trigger input to pin 2 of 555 timer form the function generator.
3. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
4. Switch on the power supply to CRO and the circuit.

5. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings along with trigger pulse.

**Result:**

Thus the Astable Multivibrators and Monostable Multivibrators using 555 timer is designed and tested.



**EX.No:**

## FREQUENCY RESPONSE OF 2nd ORDER LPF & HPF

**Aim:-**

To design and test the frequency response of a second order LPF and HPF.

**Components Required:-**

| S.No | Components | Range | Quantity |
|---|---|---|---|
| 1. | Op-amp | IC 741 | 1 |
| 2. | Resistors | | |
| 3. | Capacitor | O.01μf | 2 |
| 4. | CRO | | 1 |
| 5. | Power Supply | ± 15V | 1 |
| 6. | Probe | | 2 |
| 7. | Bread Board | | 1 |

**Theory:-**

**LPF:-**

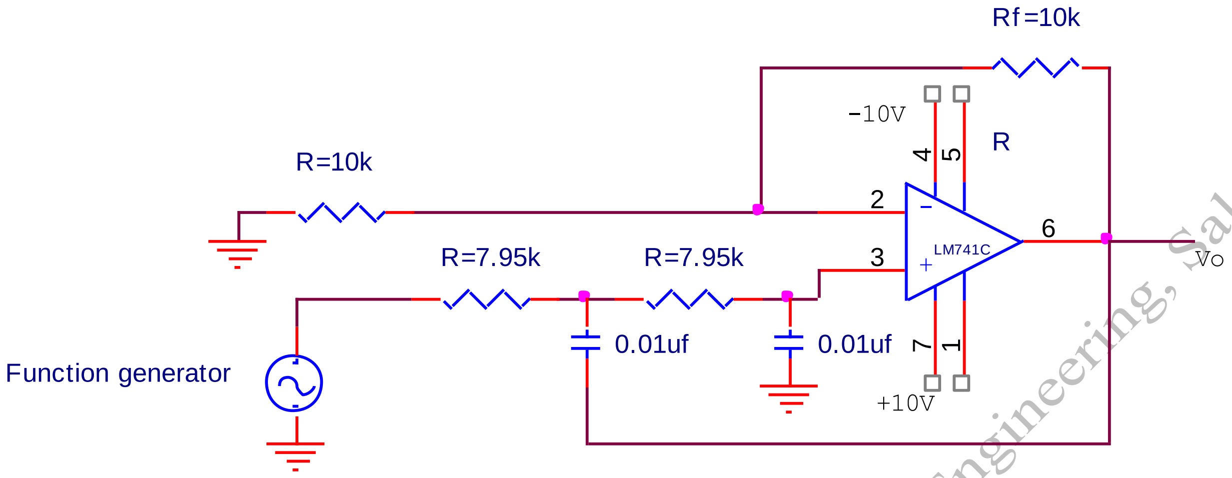
A LPF allows only low frequency signals up to a certain break-point $f_H$ to pass through, while suppressing high frequency components. The range of frequency from 0 to higher cut off frequency $f_H$ is called pass band and the range of frequencies beyond $f_H$ is called stop band.

The following steps are used for the design of active LPF.

1. The value of high cut off frequency $f_H$ is chosen.
2. The value of capacitor C is selected such that its value is $\leq 1\mu F$.
3. By knowing the values of $f_H$ and C, the value of R can be calculated using $f_H = \frac{1}{2\pi RC}$
4. Finally the values of $R_1$ and $R_f$ are selected depending on the designed pass band gain by using $A = 1 + \left(\frac{R_f}{R_1}\right)$

**Circuit Diagram:-**

**Second Order LPF:**




**Design:-**

**Second order:-**

Given frequency, $f_H$ = 2 KHz and gain =2

Let C=0.01µf

The frequency, $f_H = \dfrac{1}{2\pi\sqrt{\left(2\times10^{3}\right)\left(0.01\times10^{-6}\right)}}$

Set, $R_2 = R_3 = R$

$C_2 = C_3 = C$

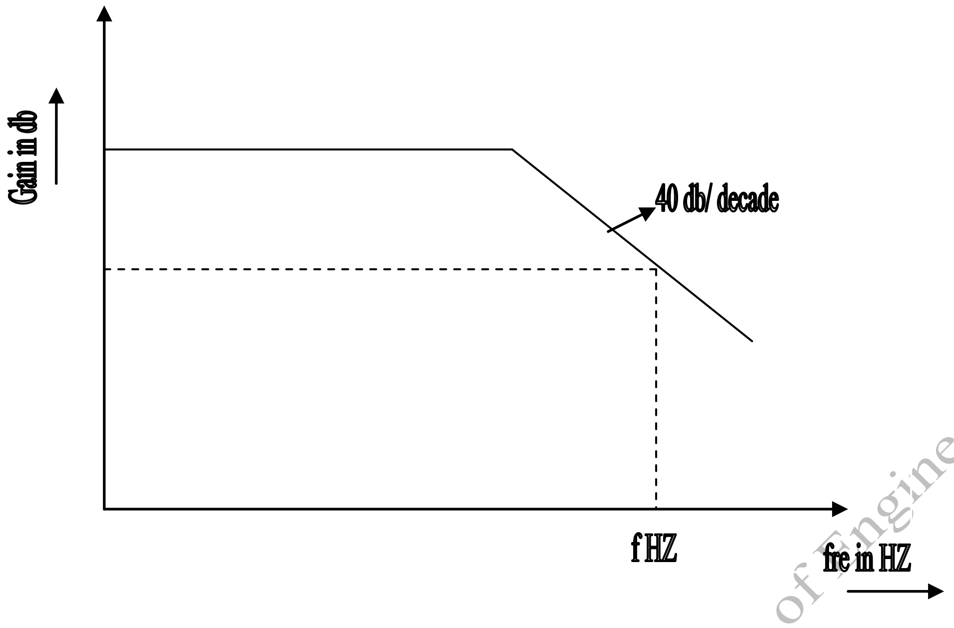
$\therefore f_H = \dfrac{1}{2\pi RC}$

**Tabulation**

**Second order LPF** Vin=1V

| S.No | Frequency (Hz) | O/p voltage(v) | Gain=Vo/Vin | Gain=20log(Vo/Vin) |
|---|---|---|---|---|
| | | | | |

**Model graph:-**

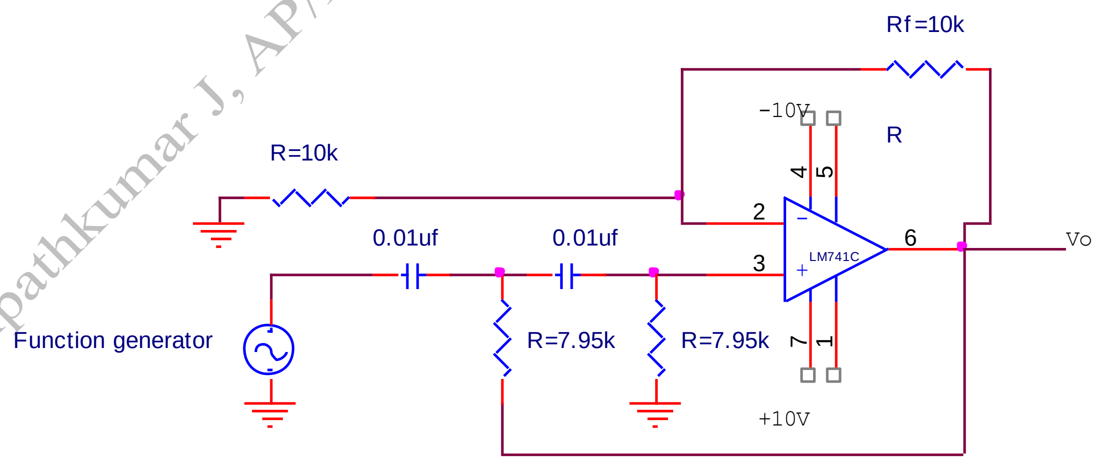



**Second order HPF:**

**Theory:-**

The high pass filter is the complement of the low pass filter. Thus the high pass filter can be obtained by interchanging R and C in the circuit of low pass configuration. A high pass filter allows only frequencies above a certain bread point to pass through and at terminates the low frequency components. The range of frequencies beyond its lower cut off frequency $f_L$ is called stop band.

**Circuit Diagram:-**
**Second Order HPF:**



**Design:-**

$$f_L = 2\mathbf{K}HZ$$

$$C = 0.01\mu F$$

$$Gain,\ Av = 2$$

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$Let\ \ R_2 = R_3 = R$$
$$C_2 = C_3 = C$$

$$R_2 = R_3 = \frac{1}{2\pi f L C}$$

$$R_2 = R_3 = 7.95 k\Omega$$

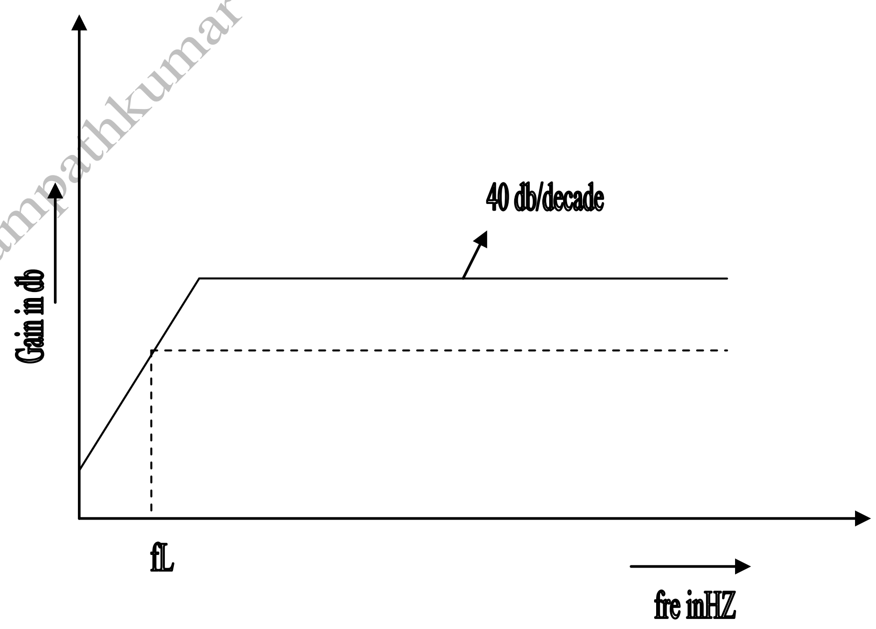
$$A = 1 + \frac{R_f}{R_1} = 2$$

$$\therefore R_f = R_1 = 10 k\Omega (given)$$

Vin=1V

| S.No | Frequency (Hz) | O/p voltage(v) | Gain=Vo/Vin | Gain=20log(Vo/Vin) |
|---|---|---|---|---|
| | | | | |

**Model graph:-**



**Procedure:-**

**LPF:-**

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

**HPF**

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

**Result:-**

Thus the second order Low pass filter and High pass filter were designed using Op-amp and its cut off frequency was determined.

**EX.No:**

## FREQENCY RESPONSE OF 2nd ORDER BSF & BPF

**Aim:-**

To design and test the frequency response of a second order LPF and HPF.

**Components Required:-**

| S.No | Components | Range | Quantity |
|---|---|---|---|
| 1. | Op-amp | IC 741 | 3 |
| 2. | Resistors | | |
| 3. | Capacitor | O.01μf, O.05μf | 2 |
| 4. | CRO | | 1 |
| 5. | Power Supply | ± 15V | 1 |
| 6. | Probe | | 2 |
| 7. | Bread Board | | 1 |

**Theory:-**

**BSF:-**

BSF is the logical inverse of band pass filter which does not allows a specified range of frequencies to pass through. It has two pass bands in the range of frequencies between 0 to $f_L$ and beyond $f_H$ . The band between $f_L$ and $f_H$ is called stop band. BSF is also called Band Reject Filter (BRF) or Band Elimination Filter (BEF).

**BPF:-**

The BPF is the combination of high and low pass filters and this allows a specified range of frequencies to pass through. It has two stop bands in range of frequencies between 0 to $f_L$ and beyond

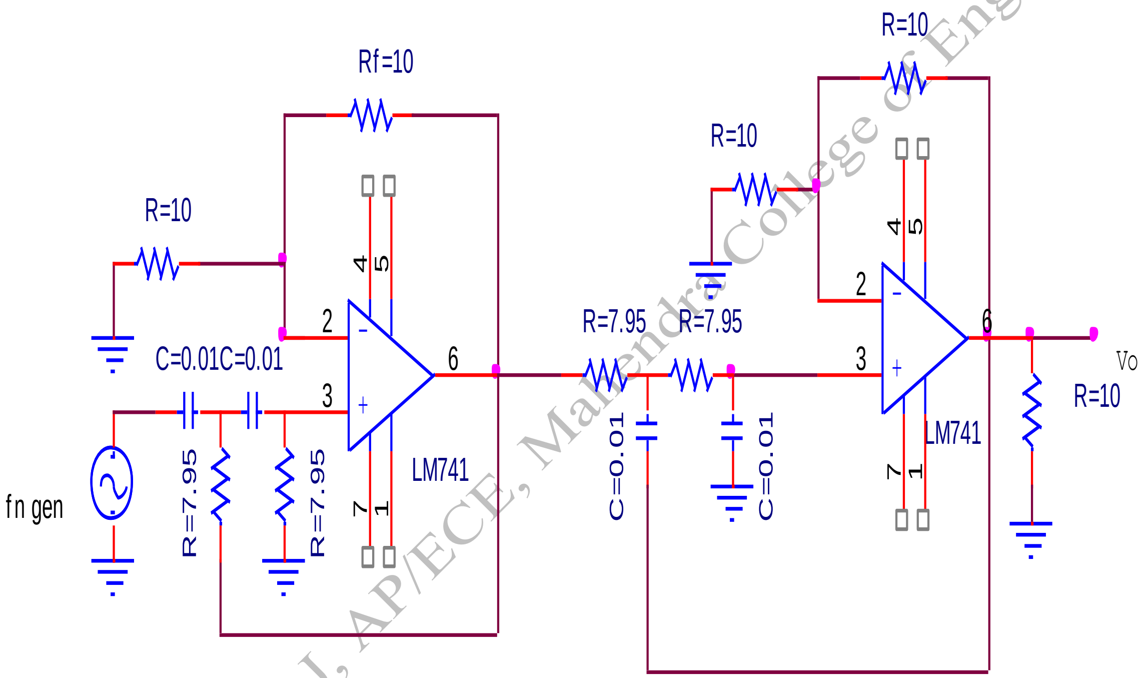
$f_H$. The band b/w $f_L$ and $f_H$ is called pass band. Hence its bandwidth is ($f_L$-$f_H$). This filter has a maximum gain at the resonant frequency ($f_r$) which is defined as

$$f_r = \sqrt{f_H f_L}$$

The figure of merit (or) quality factor Q is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{BW}$$

**Circuit Diagram:-**
**BPF**




**Design:-**
**BSF:-**

$f_H$=200Hz
$f_L$=1kHz

**Low pass section**:-

$f_H$=200Hz
Let $C^1$=0.05µf

Then,

$$R^1 = \frac{1}{2\pi f_H c^1}$$

$$R^1 = \frac{1}{2\pi(200)(0.05\times10^{-6})}$$

$$R^1 = 15.9K\Omega$$

$$C^1 = 0.05\mu f$$

**High Pass Section:-**

$$f_L = 1KHZ$$

$$C = 0.01\mu f$$

$$R = \frac{1}{2\pi f_L C}$$

$$= \frac{1}{2\pi(1\times10^{3)}(0.01\times10^{-6})}$$

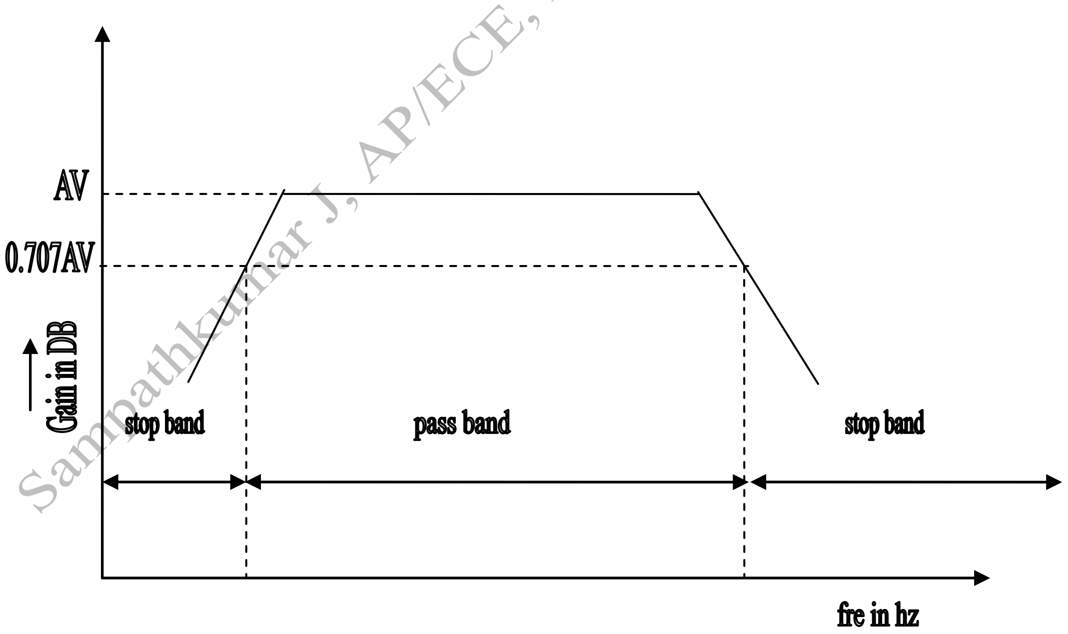
$$R = 15.9K\Omega$$

Gain, Av=2 for each section

$$\therefore R_1 = R_f = R_1^1 = R_f^1 = 10K\Omega$$

**Model graph:-**

**BPF:**



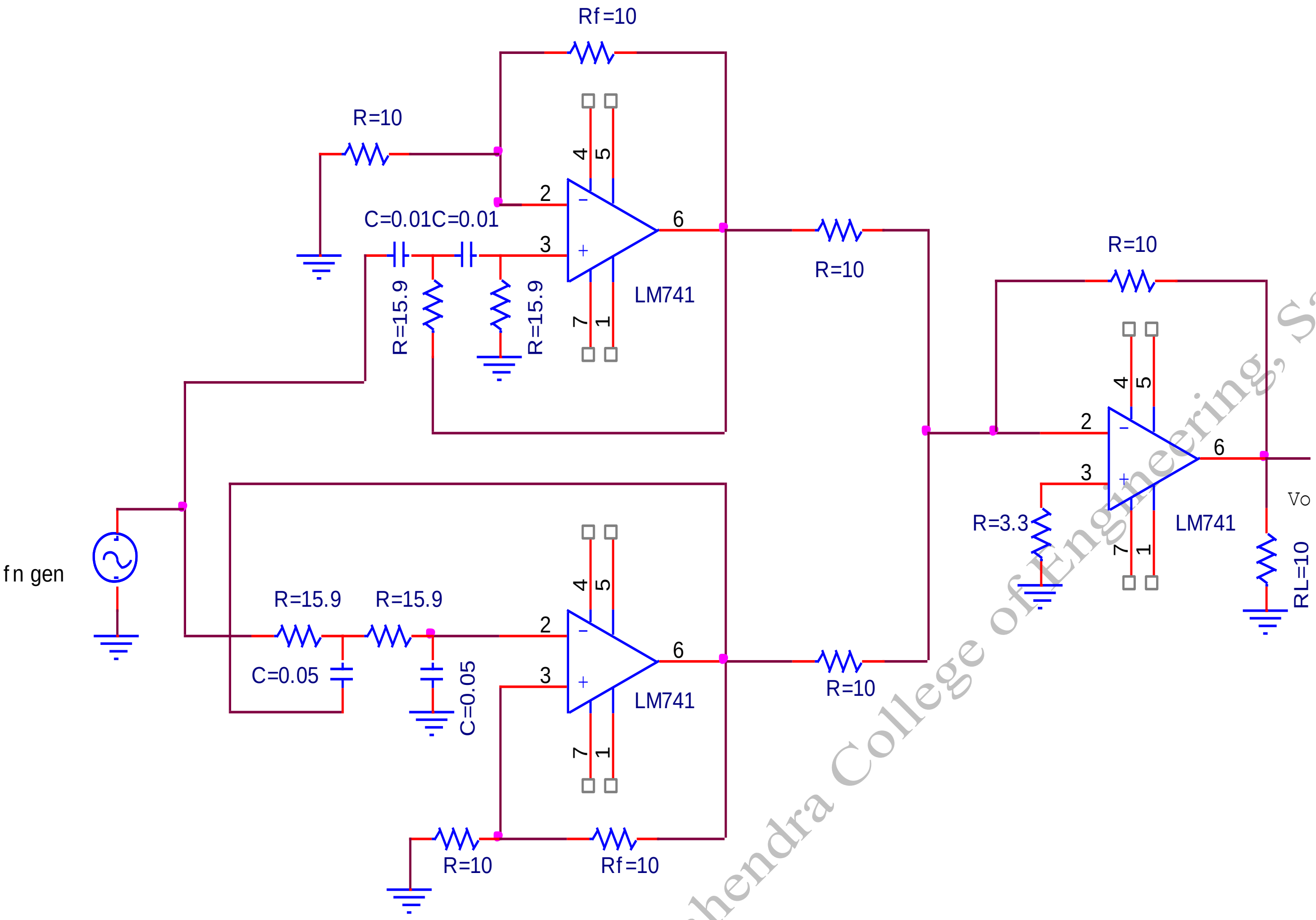
**Tabulation:-**

**BPF** Vin=50mv

| S.No | Frequency (Hz) | Vo(volts) | Gain=20log(Vo/Vin) |
|---|---|---|---|
| | | | |

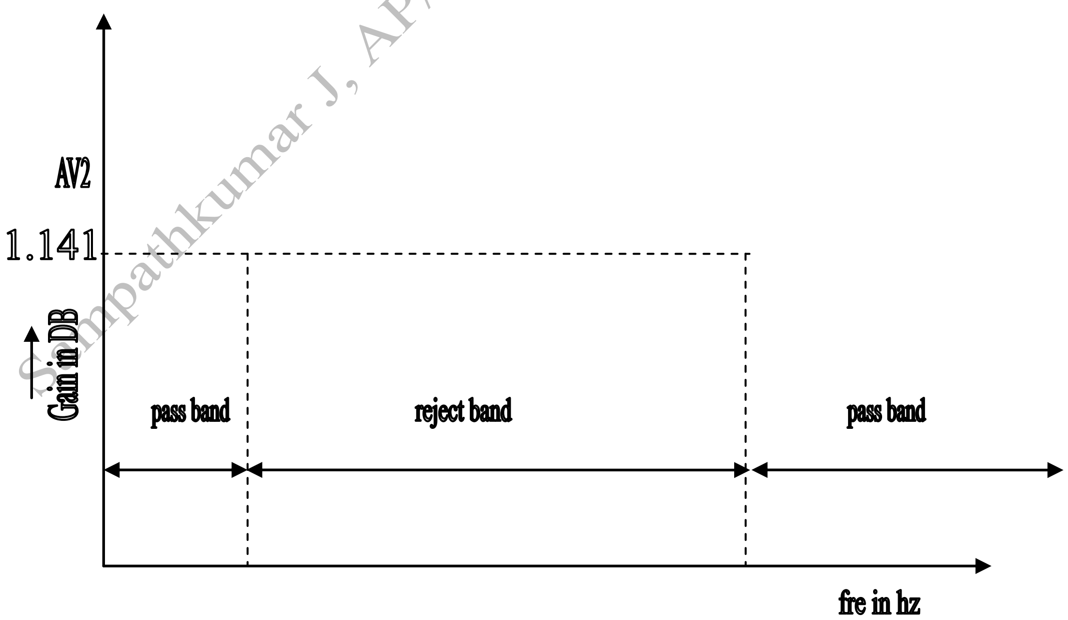
**Circuit Diagram:-**

**BSF**




**Model graph:-**

**BSF:-**



**Tabulation:-**

**BSF**

Vin=50mv

| S.No | Frequency (Hz) | Vo(volts) | Gain=20log(Vo/Vin) |
|---|---|---|---|
| | | | |

**Procedure:**
**BSF,BPF:-**

1. The input signal is connected to the circuit from the signal generator.
2. The input and output signals are connected to the filter.
3. The suitable voltage is selected.
4. The correct polarity is checked.
5. The steps are repeated.

**Result:-**

Thus the frequency response of second order BPF and BSF filter was designed and tested.

**EXP.NO.:**

## OSCILLATORS USING OPERATIONAL AMPLIFIER

**Aim:**

To design the following sine wave oscillators

a) Wein Bridge Oscillator with the frequency of 1 KHz.
b) RC Phase shift oscillator with the frequency of 200 Hz.

**Components Required:**

| S.No | Components | Range | Quantity |
|---|---|---|---|
| 1. | Op-amp | IC 741 | 1 |
| 2. | Dual trace supply | (0-30) V | 1 |
| 3. | Function Generator | (0-2) MHz | 1 |
| 4. | Resistors | | |
| 5. | Capacitors | | |
| 6 | CRO | (0-30) MHz | 1 |
| 7 | Probes | -- | -- |

**Equations Related to the Experiments:**

a) Wein Bridge Oscillator

Closed loop gain $A_v = (1+R_f/R_1) = 3$

Frequency of Oscillation $f_a = 1/(2\pi RC)$

b) RC Phase shift Oscillator:

Gain $A_v = [R_f/R_1] = 29$

Frequency of oscillation $f_a = 1\sqrt{6} * 2 * \pi * RC$

1) **Wein Bridge Oscillator:**

**Design:**

Gain required for sustained oscillation is $A_v = 1/\beta = 3$

(PASS BAND GAIN) (i.e.) $1+R_f/R_1 = 3$

$\therefore R_f = 2R_1$

Frequency of Oscillation $f_o = 1/2\pi$ R C

Given $f_o$ = 1 KHz

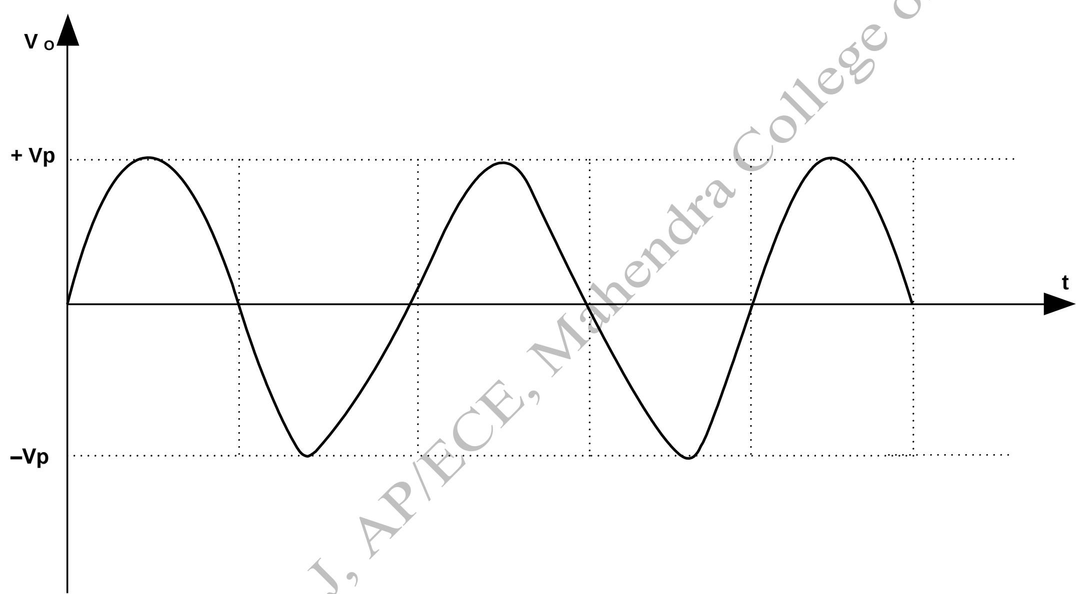
Let C = 0.05 μF

$\therefore$ R = 1/2 π $f_o$C

R = 3.2 KΩ

Let R1 = 10 KΩ $\therefore$ Rf = 2 * 10 KΩ

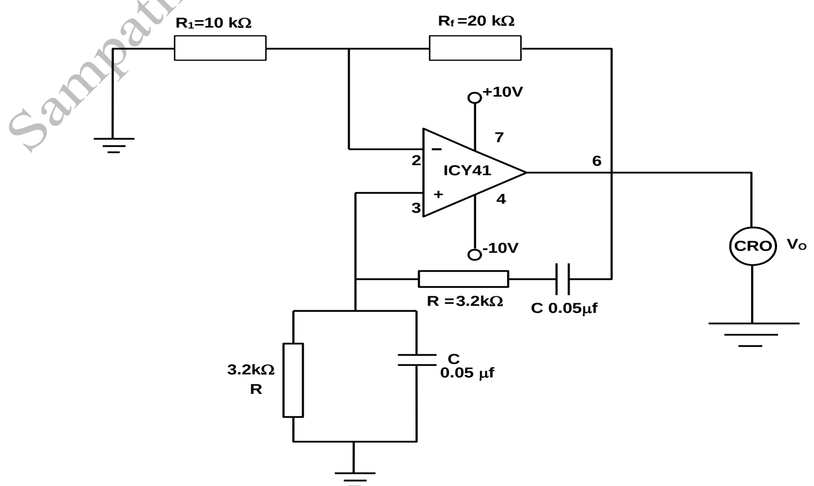
**Model Graph:**




**Procedure:**

1. Connect the components as shown in the circuit 5.1

**Circuit 5.1:**



2. Switch on the power supply and CRO.
3. Note down the output voltage at CRO.
4. Plot the output waveform on the graph.
5. Redesign the circuit to generate the sine wave of frequency 2KHz.
6. Compare the output with the theoretical value of oscillation.

**Observation:**

Peak to peak amplitude of the output = Volts.
Frequency of oscillation = Hz.

**2) RC Phase Shift Oscillators:**

**Design:**

Frequency of oscillation fo = 1/(√6*2*Π*RC)

Av = [Rf/R1] = 29

$R_1 = 10\ R$

$R_f = 29\ R_1$

Given fo = 200 Hz.

Let C = 0.1μF

$$R = 1/\left(\sqrt{6} * 2\,\pi * fo * C\right)$$

$$= 1/\left(\sqrt{6} * 2 * \pi * 200 * 0.1 * 10^{-6}\right)$$

$$= \qquad K\Omega$$

To prevent the loading of amplifier by RC network, $R1 \geq 10R$

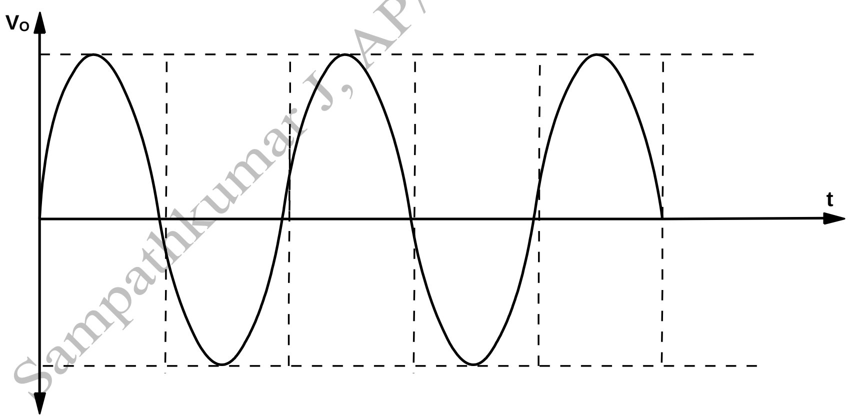
$$\therefore R1 = 10 * ------ = K\Omega$$

$$\text{Since } Rf = 29R1$$

$$Rf = 29 * ------$$

$$= \qquad M\Omega$$

**Model Graph:**

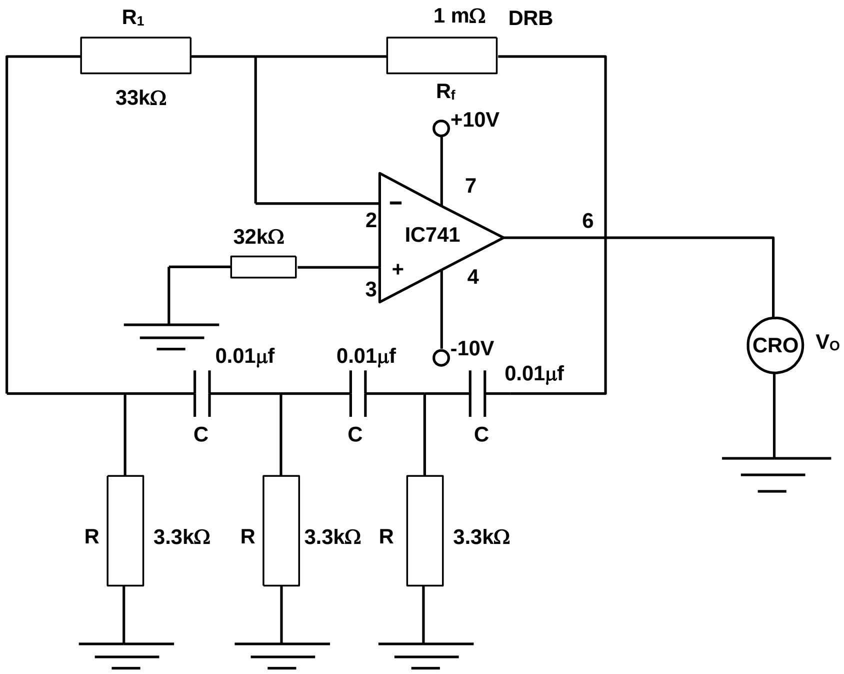





**Procedure:**

1. Connect the circuits as shown in the circuit 5.2
2. Switch on the power supply.

**Circuit 5.2:**




3. Note down the output voltage on the CRO.
4. Plot the output waveforms on the graph.
5. Redesign the circuit to generate the sine wave of 1 KHz.
6. Plot the output waveform on the graph.
7. Compare the practical value of the frequency with the theoretical value.

**Observation:**

Peak to peak amplitude of the sine wave = Volts

Frequency of Oscillation (obtained) = Hz

**Result:**

Thus wien bridge oscillator and RC Phase shift oscillator was designed using op-amp and tested.

**EXP.NO.: VOLTAGE REGULATION USING IC LM723**

**AIM :**

To design a high current, low voltage and high voltage linear variable dc regulated power supply and test its line and load regulation.

**COMPONENTS REQUIRED :**

| S.NO | COMPONENTS | SPECIFICATION | QUANTITY |
|---|---|---|---|
| 1. | Transistors | TIP122,2N3055 | 1 each |
| 2. | Integrated Circuit | LM723 | 1 |
| 3. | Digital Ammeter | ( 0 – 10 ) A | 1 |

| | | | |
|---|---|---|---|
| 4. | Digital Voltmeter | ( 0 – 20 ) V | 1 |
| 5. | Variable Power Supply | ( 0 – 30 ) V-2A | 1 |
| 6. | Resistors | 300Ω,430Ω,1KΩ,678KΩ,678Ω<br>1Ω | 1 each<br>2 |
| 7. | Capacitors | 0.1μF,100pF | 1 each |
| 9. | Rheostat | ( 0 – 350 ) Ω | 1 |

**CIRCUIT DIAGRAM : Low Voltage Regulator**

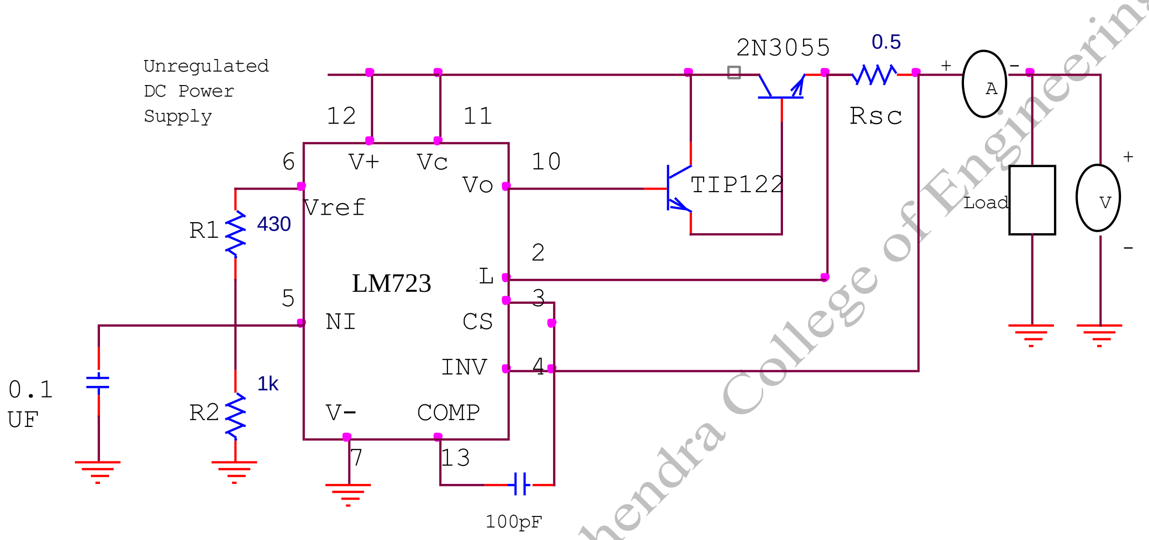



Fig. 1.1

**DESIGN:**

Output voltage → $V_O$

Reference voltage→ Vref

Rprotect → Minimum Resistance to protect the output from short circuit.

**Low Voltage Regulator :**

**<u>Given : Vo=5V, Vref = 7.15 V</u>**

To calculate R1, R2 ,R3 and Rsc.

Vo = Vref ( R2 / ( R1 + R2 ) )

5 / 7.15 = ( R2 / ( R1 + R2 ) )

( R1 + R2 ) 0.699= R2

0.699R1 = 0.301 R2 , R1 = 0.4306 R2

Select **R2 = 1 KΩ**

R1 = 1 KΩ * 0.4306 = 430Ω

**<u>R1 = 430Ω</u>**

R3 = R1 * R2 / ( R1 + R2) , R3 = 430.6 *1000 /(430.6+1000 )

**R3 = 300Ω**

$Rsc = V_{sense} / I_{limit} = 0.5 / 1A = 0.5\Omega$ , **Rsc = 0.5Ω**

## CIRCUIT DIAGRAM : High Voltage Regulator :

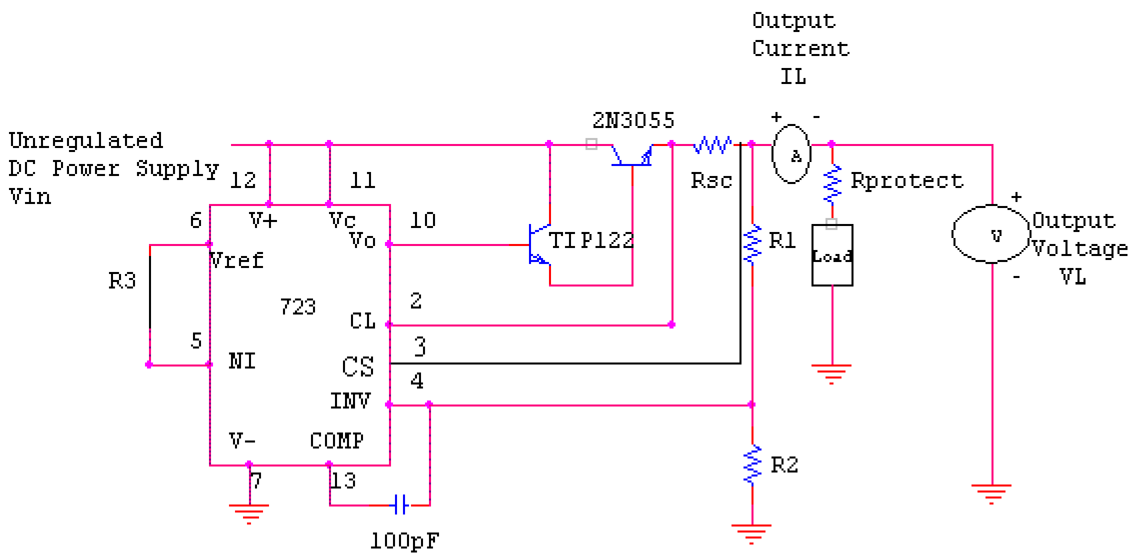



Fig. 1.2

### High Voltage Regulator :

<u>**Given : Vo=12V, Vref = 7.15 V**</u>

To calculate R1, R2 ,R3 and Rsc.

Vo = Vref ( 1 + (R1 / R2) )

12 / 7.15 = 1+ (R1 / R2)

(12 / 7.15) - 1 = (R1 / R2)

(R1 / R2) = 0.678

Select **R2 = 1 KΩ**

R1 = 1 KΩ * 0.678 = 678Ω

**R1= 678Ω**

$Rsc = V_{sense} / I_{limit} = 0.5 / 1A = 0.5\Omega$

**Rsc = 0.5Ω**

### Tabulation of the Measurements :

**LOW VOLTAGE REGULATOR :**

**Line Regulation :**

| **S.No.** | Load Resistance $R_{L1}$ = | | Load Resistance $R_{L2}$ = | | Load Resistance $R_{L3}$ = | |
|---|---|---|---|---|---|---|
| | Input Voltage Vin(Volts) | Output Voltage $V_L$(Volts) | Input Voltage Vin(Volts) | Output Voltage $V_L$ (Volts) | Input Voltage Vin(Volts) | Output Voltage $V_L$ (Volts) |
| | | | | | | |

**Load Regulation :**

| S.No. | Input Voltage $V_{in1}$ = | | Input Voltage $V_{in2}$ = | | Input Voltage $V_{in3}$ = | |
|---|---|---|---|---|---|---|
| | Output Current $I_L$ ( A ) | Output Voltage $V_L$ (Volts) | Output Current $I_L$ ( A ) | Output Voltage $V_L$ (Volts) | Output Current $I_L$ ( A ) | Output Voltage $V_L$ (Volts) |
| | | | | | | |

**HIGH VOLTAGE REGULATOR :**

**Line Regulation :**

| S.No. | Load Resistance $R_{L1}$ = | | Load Resistance $R_{L2}$ = | | Load Resistance $R_{L3}$ = | |
|---|---|---|---|---|---|---|
| | Input Voltage Vin(Volts) | Output Voltage $V_L$(Volts) | Input Voltage Vin(Volts) | Output Voltage $V_L$ (Volts) | Input Voltage Vin(Volts) | Output Voltage $V_L$(Volts) |
| | | | | | | |

**Load Regulation :**

| S.No. | Input Voltage $V_{in1}$ = | | Input Voltage $V_{in2}$ = | | Input Voltage $V_{in3}$ = | |
|---|---|---|---|---|---|---|
| | Output Current $I_L$ ( A ) | Output Voltage $V_L$(Volts) | Output Current $I_L$ ( A ) | Output Voltage $V_L$(Volts) | Output Current $I_L$ ( A ) | Output Voltage $V_L$(Volts) |
| | | | | | | |

**Calculation of % Voltage Regulation :**

% Voltage Regulation = ( $V_{dc}$ ( NL ) - $V_{dc}$ ( FL ) ) / $V_{dc}$ ( FL )

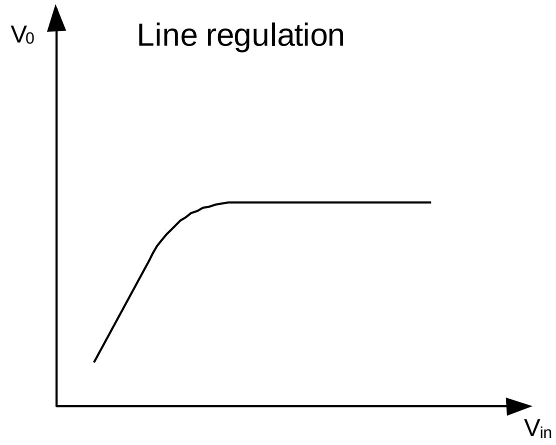
$V_{dc}$ ( NL ) = D.C. output voltage on no load

$V_{dc}$ ( FL ) = D.C. output voltage on full load

**Model Graph :**

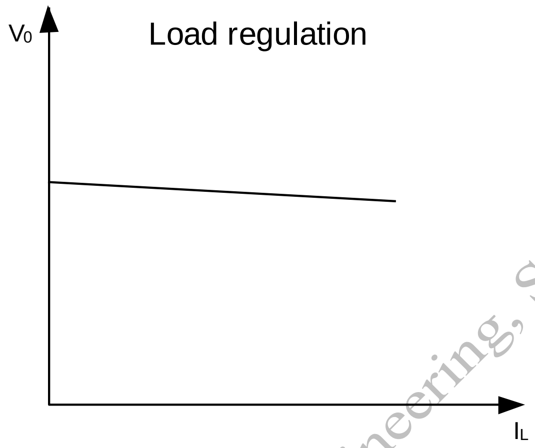
**Line Regulation :** 

**Input Voltage Vs Output Voltage :**




**Load Regulation :**

**Output Current Vs Output Voltage**




**PROCEDURE :**

**LOW VOLTAGE REGULATOR :**

**Line Regulation :**

1. Give the circuit connection as per the circuit diagram shown in Fig 1.1.
2. Set the load Resistance to give load current of 0.25A.
3. Vary the input voltage from 7V to 18V and note down the corresponding output voltages.
4. Similarly set the load current ( $I_L$ ) to 0.5A & 0.9A and make two more sets of measurements.

**Load Regulation :**

1. Set the input voltage to 10V.

2. Vary the load resistance in equal steps from 350Ω to 5Ω and note down the corresponding output voltage and load current.

3.Similarly set the input voltage ( Vin ) to 14V & 18V and make two more sets of measurements.

**Lab Report :**

1.Plot the line regulation by taking Input Voltage (Vin) along X-axis and Output Voltage ($V_L$) along Y-axis for various load currents.

2.Plot the load regulation by taking load current ($I_L$) along X-axis and Output Voltage ($V_L$) along Y-axis for various input voltages.

3.Calculate its % Voltage Regulation using the formula.



**HIGH VOLTAGE REGULATOR :**

**Line Regulation :**

1.Give the circuit connection as per the circuit diagram shown in Fig 1.2.

2.Set the load Resistance to give load current $I_L$ of 0.25A.

3.Vary the input voltage from 7V to 18V and note down the corresponding output voltages.

4.Similarly set the load current ( $I_L$ ) to 0.5A & 0.9A and make two more sets of measurements.

**Load Regulation :**

1. Set the input voltage to 10V.

2. Vary the load resistance in equal steps from 350Ω to 15Ω and note down the corresponding output voltage and load current.

3.Similarly set the input voltage ( Vin ) to 14V & 18V and make two more sets of measurements.

**Lab Report :**

1.Plot the line regulation by taking Input Voltage (Vin) along X-axis and Output Voltage ($V_L$) along Y-axis for various load currents.

2.Plot the load regulation by taking load current ($I_L$) along X-axis and Output Voltage ($V_L$) along Y-axis for various input voltages.

3.Calculate its % Voltage Regulation using the formula.

**Result :**

Thus the line and load regulation of a high current, low voltage and high voltage linear variable dc regulated power supply was designed and tested.

| S.No | Low Voltage Regulator | High Voltage Regulator |
|---|---|---|
| % Voltage Regulation | | |

## VOLTAGE REGULATION USING IC 317

**AIM:**

To design, construct and test voltage regulator using IC 317.

**APPARATUS REQUIRED:**

i. IC 317
ii. Resistors, capacitors
iii. RPS

**THEORY:**

One of the most popular variable voltage regulators is the IC 317 regulator. The LM 317 is an adjustable three terminal positive voltage regulator. They are capable of supplying output current of 0.1A to 1.5A, over a range of 1.2V to 37V.

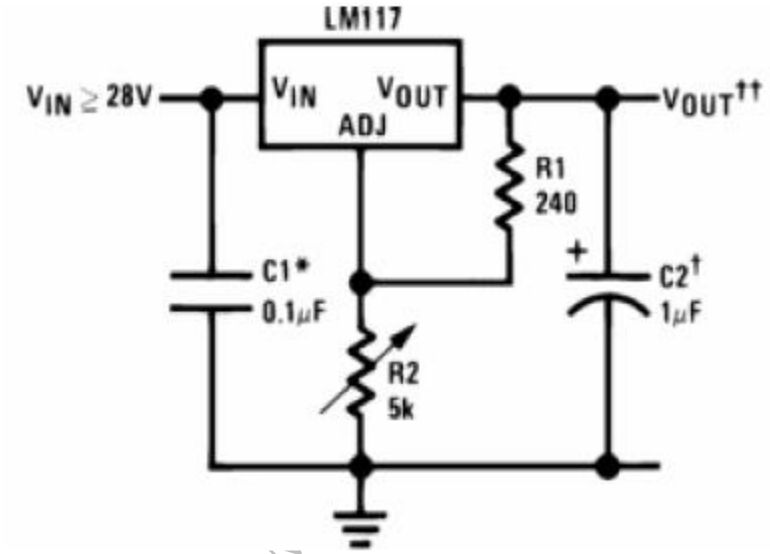
The basic circuit connection is as shown in the diagram. The LM 317 needs two resistors R1, R2 for setting the output voltage. Usually the input capacitor is of disc type and the output is of electrolytic type to improve the transient response. The unregulated input is applied at Vi , which is normally 2V
more than the required output voltage.

When the circuit is connected as shown the value of Vref =1.25V, between the output and the adjustable terminals. This voltage is dropped across R1, driving a current I1= Vref/R1. So the net current flowing through R2 is I1+IADJ. But as IADJ is very small, VO=Vref(1+R2/R1) where the reference voltage is 1.25V

## DESIGN:

Let capacitors C1=0.1uF and C2=1uF.
If resistor R1=240 ohms and if R2 =1000 ohms;
Then regulated output=1.25*(1+R2/R1)=6.46 volts
If a variable resistor is used in the place of R2, we can get can adjustable output voltage.

**CIRCUIT DIAGRAM:**




**PROCEDURE:**

i. Give the circuit connections as per the circuit diagram.
ii. By varying the input voltage observe the output voltage.
iii. Now change the resistor values to get a different VO.
iv. Once again by varying the supply observe the output.
v. Draw the regulation curve.

**RESULT:**

Thus the voltage regulator using LM 317 is designed, constructed and tested.



## FREQUENCY MULTIPLIER USING PLL IC

**AIM:**

To study the operation of NE 565 PLL as a frequency multiplier.

**APPARATUS REQUIRED:**

i. RPS
ii. Resistors, Capacitors
iii. IC NE565, IC 7490

iv. Transistor 2N3391
v. Breadboard, connecting wires.

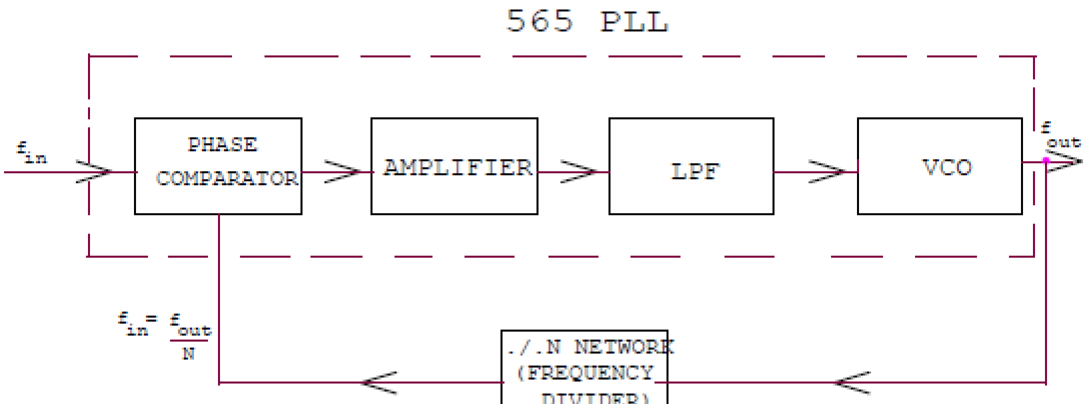
**THEORY:**

Figure shows the block diagram of a frequency multiplier using the 565 PLL. The frequency counter is inserted between the VCO and the phase comparator. Since the output of the divider is locked to the input frequency $f_{IN}$, the VCO is actually running at a multiple of the input frequency.

The desired amount of multiplication can be obtained by selecting a proper divide by N network, where N is an integer. For example, to obtain the output frequency $f_{OUT} = 5\ f_{IN}$, a divide by N = 5 network is needed. The 4 bit binary counter (7490) is configured as a divide by 5 circuit. The transistor Q is used as a driver stage to increase the driving capability of the NE 565. C3 is used to eliminate possible oscillation. C2 should be large enough to stabilize the VCO frequency.

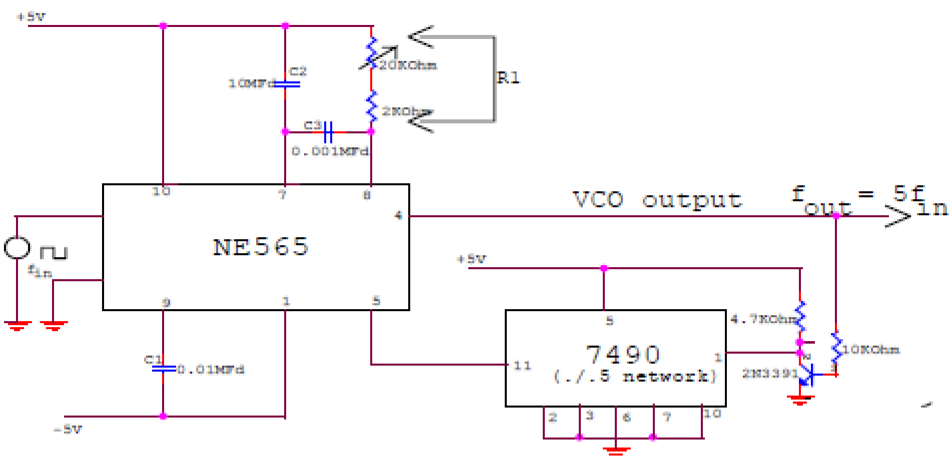
**PROCEDURE:**

1. Connect the circuit as shown in figure.
2. Adjust the signal generator so that Vi =1V p-p square wave at 500Hz
3. The free running frequency $f_{OUT}$ of VCO is varied by adjusting R1 and C1 and the output frequency is determined and it should be 5 times the input frequency.
4. Determine the output frequency for different input frequency of 1KHz and 1.5 KHz.




**CIRCUIT DIAGRAM:**

**FREQUENCY MULTIPLIER CIRCUIT**



| $t_{low}$ (ms) | | $t_{high}$ (ms) | | **Frequency (Hz)** | |
|---|---|---|---|---|---|
| theoretical | Practical | theoretical | practical | theoretical | practical |
| | | | | | |

**RESULT:**

The frequency multiplier using PLL principle is studied and the output waveform is observed.